NON IDEAL IV CHARACTERISTICS

The non- ideal Iv effect include the following:-

1) Velocity saturation & mobility degradation.
2) Channel length modulation
3) Body effect
4) Sub threshold condition
5) Junction Leakage
6) Tunneling
7) Temperature dependence
8) Geometry Dependence.

Velocity saturation and mobility degradation:-

- Carrier drift velocity and current increase linearly with the lateral field E lat = V_{ds}/ L between source and drain.
- At high field strength, drift velocity rot off due to carrier scattering and usually saturates at V sat .
- Without velocity saturation the saturation current is

$$I_{ds} = \mu C_o \times \frac{W}{L} \frac{(V_{gs} - V_{ds})^2}{2}$$

- If the transistor is completely Velou saturated $V = V_{sat}$ and saturation current become .

- $I_{ds} = C_0 \times W (V_{gs} - V_t) V_{sat}$ without velocity saturation .

$$I_{ds} = \begin{cases} 0 & ; V_{gs} < V_t \quad \text{cut off} \\ I_{dsat} = V_{ds} & ; V_{ds} < V_{dsat} \quad \text{linear} \\ I_{dsat} & ; V_{ds} > V_{dsat} \quad \text{saturation.} \end{cases}$$

Where $I_{dsat} = P_c \frac{\beta}{2} (V_{gs} - V_t)^2 V_{dsat} = P_v (V_{gs} - V_t) a/2$.

- As channel length becomes shorter, the lateral field increases and transistors become more velocity saturated, and the supply voltage is held constant.

Channel Length Modulation:-

- Ideally Ids is independent of V_{ds} in saturation.
- The reverse biased p-n junction between the drain and body forms a depletion region with a width L_d that increases with V_{db}.
- The depletion region effectively shortens the channel length to Leff =L-Ld.
- Imagine that the source voltage is close to the body voltage. Increasing V_{ds} decreases the effective channel length. Shorter length results in higher current. Thus Ids increases with V_{ds} in saturation as shown below.

In saturation region

$$Ids = \beta \frac{(Vgs - V_t)2}{2} (1+ \lambda V_{ds}$$

Where λ = Channel length modulation facto

Transistor has four terminals named gate, source, drain and body. The potential difference between the source and body V_{sb} affects the threshold voltage.

$$V_t = V_{to} + \gamma \left(\sqrt{p_s + V_{sb}} - \sqrt{\varphi_s} \right)$$

Where

V_{to} = Threshold Voltage when the source is at the body potential

φ_s = Surface Potential at threshold = $2vT \ln \frac{Nd}{Ni}$

V_{sb} = Potential difference between the source and body.

Sub threshold condition:

- Ideally current flows from source to drain when $V_{gs} > V_t$. In real transistor, current does not abruptly cut off below threshold, but rather drops off exponentially as

$$I_{ds} = I_{dso} e^{\frac{V_{gs} - V_t}{V_t}} [1 - e^{\frac{V_{ds}}{V_t}}]$$

This is also called as leakage and often this results in underwired current when a transistor is normally OFF. I_{dso} is the current at threshold and is dependent on process and device geometry

Applications:-

- This is used in very low power analog circuit
- This is used in dynamic circuits and OR AM

Advantage:

1) Leakage increases exponentially as V_t decreases or as temperature rises.

Disadvantages:

1) It becomes worse by drain induced barrier lowering in which a positive V_{ds} effectively reduces V_t. This effect is especially pronounced in short channel transistors.

Junction Leakage:

- The P-n junction between diffusion and the substrate or well form diodes are shown below.
- The substrate and well are tied to GND or V_{DD} to ensure that these diodes remain reverse biased.

The reverse biased diodes still conduct a small amount of current I o. $I_D = I_s [e \underline{V_D} -1]V_T$

Where

I_D = diode current

I_s = diode reverse- biased saturation current that depends on doping levels and on the area and perimeter of the diffusion region.

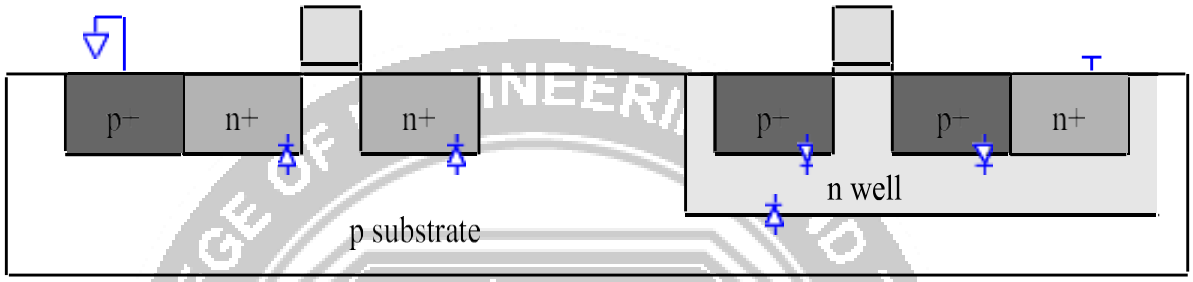

Figure 1.3.1 : Junction Leakage

[Source: Sung-Mo kang, Yusuf leblebici, Chulwoo Kim ―CMOS Digital Integrated Circuits:Analysis & Design….]

Tunneling :

Based on quantum mechanics, we see that the is a finite probability that carriers will tunnel through the gate oxide. This results in gate leakage current flowing into the gate. The probability of tunnelling drops off exponentially with oxide thickness.

- Large tunnelling currents impact not only dynamic nodes but also quiescent power consumption and thus may limit oxide thickness tor.
- Tunnelling can purposely be used to create electrically erasable memory devices. Different dielectrics may have different tunneting properties.

Temperature Dependance:

Temperature influences the characteristics of transistors. Carrier mobility decreases with temperature.

$$\mu (T) = \mu (T_r) (\underline{T})^{-k} \mu Tr$$

- Junction leakage increases with temperature because. I_s is strongly temperature dependent . The combined temperature effect is shown below.

Where on current decreases and OFF current increases with temperature.

The figure below shows how the On current I_{dsat} decreases with temperature. Circuit performance is worst at high temperature, called negative temperature

coefficient.

- Circuit performance an be improved by cooling . Natural convection, fans with heat sink, water cooling thin flim refrigerators, and liquid nitrogen can be used as cooling.

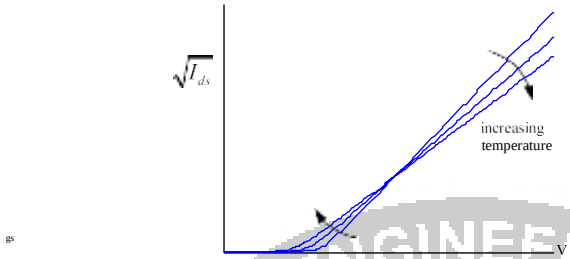

Figure 1.3.2 : Temperature Dependance

[Source: Sung-Mo kang, Yusuf leblebici, Chulwoo Kim —CMOS Digital Integrated Circuits:Analysis & Design….]

Advantages of Operating at low temperature:

1) velocity saturation occurs at higher fields providing more current.
2) For high mobility , power is saved.
3) Wider depletion region results in less junction capacitance.

Geometry Dependance:

- The layout designer draws transistors with width and length ^{W} drawn and L drawn. The actual gate dimensions may differ by factors X_w andX_L.
- The source and drain trends to diffuse later under the gate by L_{Di} producing a shorter effective between source and drain.

$$Leff = L_{drawn} + X_L - 2_{LP}$$

$$Weff = W_{drawn} + X_W - 2w_D$$

Long transistors experience less channel length modulation. In a process blow 0.25 μm the effective length of the transistor depends on the orientation of the transistor.

Ideal I-V Characteristics Of a Nmos and Pmos Device

MOS transistors have three regions of operation:

_ Cutoff or subthreshold region

_ Linear region

_ Saturation region

The current and voltage (I-V) for an nMOS transistor in each of these regions. The model assumes that the channel length is long enough that the lateral electric field (the field between source and drain) is relatively low, which is no longer the case in nanometer devices. This model is variously known as the *long-channel, ideal, first-order,* or *Shockley* model. Subsequent sections will refine the model to reflect high fields, leakage, and other nonidealities. The long-channel model assumes that the current through an OFF transistor is 0. When a transistor turns ON (*Vgs* > *Vt*), the gate attracts carriers (electrons) to form a channel. The electrons drift from source to drain at a rate proportional to the electric field between these regions. Thus, we can compute currents if we know the amount of charge in the channel and the rate at which it moves. We know that the charge on each plate of a capacitor is *Q* = *CV*. Thus, the charge in the channel *Q*channel is

$$Q_{channel}=C_g(V_{gs}-V_t)$$

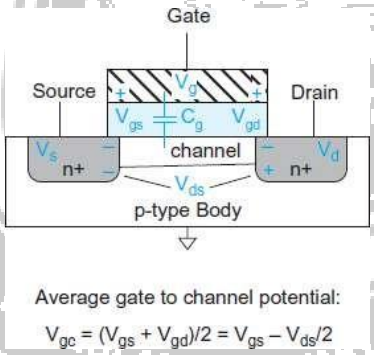

Figure 1.3.3: Ideal I-V Characteristics

[Source: Sung-Mo kang, Yusuf leblebici, Chulwoo Kim ―CMOS Digital Integrated Circuits:Analysis & Design….]

where *Cg* is the capacitance of the gate to the channel and *Vgc* - *Vt* is the amount of voltage attracting charge to the channel beyond the minimum required to invert from p to n. The gate voltage is referenced to the channel, which is not grounded. If the source is at *Vs* and the drain is at *Vd* , the average is *Vc* = (*Vs* + *Vd*)/2 = *Vs* + *Vds* /2. Therefore, the mean difference between the gate and channel potentials *Vgc* is *Vg* – *Vc* = *Vgs* – *Vds* as shown in Figure.

We can model the gate as a parallel plate capacitor with capacitance proportional to area

over thickness. If the gate has length *L* and width *W* and the oxide thickness is *t*ox, as shown in below Figure, the capacitance is

$C_g=\varepsilon ox(WL/t_{ox})=CoxWL$

where εox is the permittivity of free space, 8.85 × 10–14 F/cm, and the permittivity of SiO2 is *k*ox = 3.9 times as great. Often, the ox/*t*ox term is called *C*ox, the capacitance per unit area of the gate oxide.

Each carrier in the channel is accelerated to an average velocity, *v*, proportional to the lateral electric field, i.e., the field between source and drain. The constant of proportionality μ is called the *mobility*.

$$v = \mu E$$

The time required for carriers to cross the channel is the channel length divided by the carrier velocity: *L*/*v*. Therefore, the current between source and drain is the total amount of charge in the channel divided by the time required to cross

$$I_{ds} = \frac{Q_{channel}}{L/v}$$
$$= \mu C_{ox} \frac{W}{L}\left(V_{gs} - V_t - V_{ds}/2\right)V_{ds}$$
$$= \beta\left(V_{GT} - V_{ds}/2\right)V_{ds}$$

$$\beta = \mu C_{ox} \frac{W}{L};\ V_{GT} = V_{gs} - V_t$$

The term *Vgs* – *Vt* arises so often that it is convenient to abbreviate it as *VGT* .

$$K' = \mu C\text{ox}$$

If *Vds* > *V*dsat *VGT*, the channel is no longer inverted in the vicinity of the drain; we say it is pinched off. Beyond this point, called the *drain saturation voltage*, increasing the drain voltage has no further effect on current. Substituting *Vds* = *V*dsat at this point of maximum current in above eqn, we find an expression for the saturation current that is independent of *Vds*.

$Ids=(\beta/2)V^2_{GT}$

This expression is valid for *Vgs* > *Vt* and *Vds* > *V*dsat . Thus, long-channel MOS transistors are said to exhibit *square-law behavior* in saturation. Two key figures of merit for a transistor are *I*on and *I*off. *I*on (also called *I*dsat) is the ON current, *Ids*, when *Vgs* = *Vds* = *VDD*. *I*off is the OFF current when *Vgs* = 0 and *Vds* = *VDD*. According to

Below fig shows the I-V characteristics for the transistor. According to the first-order model, the current is zero for gate voltages below *Vt*. For higher gate voltages, current increases linearly with *Vds* for small *Vds* . As *Vds* reaches the saturation point *V*dsat = *VGT*, current rolls off and eventually becomes independent of *Vds* when the transistor is saturated. We will later see that the Shockley model overestimates current at high voltage because it does not account for mobility degradation and velocity saturation caused by the high electric fields.

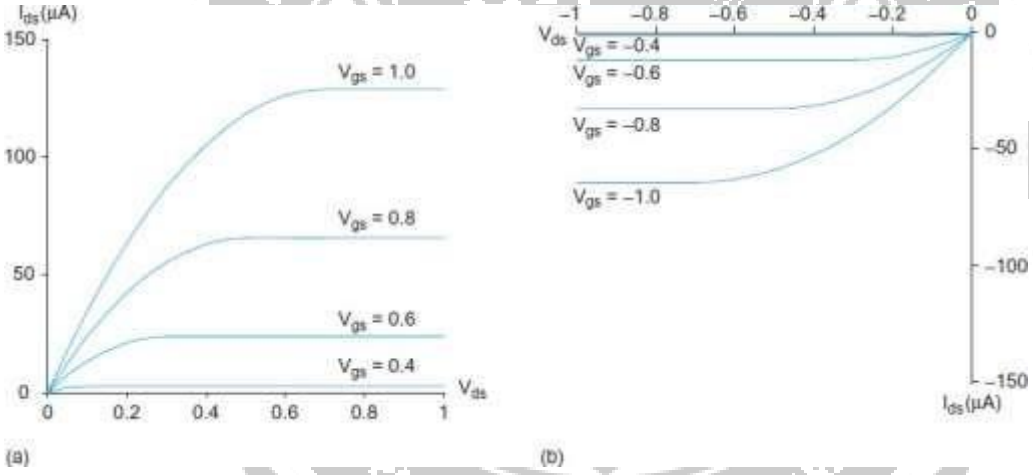

Figure 1.3.4 :I-V Characteristics

[Source: Sung-Mo kang, Yusuf leblebici, Chulwoo Kim ―CMOS Digital Integrated Circuits:Analysis & Design…]