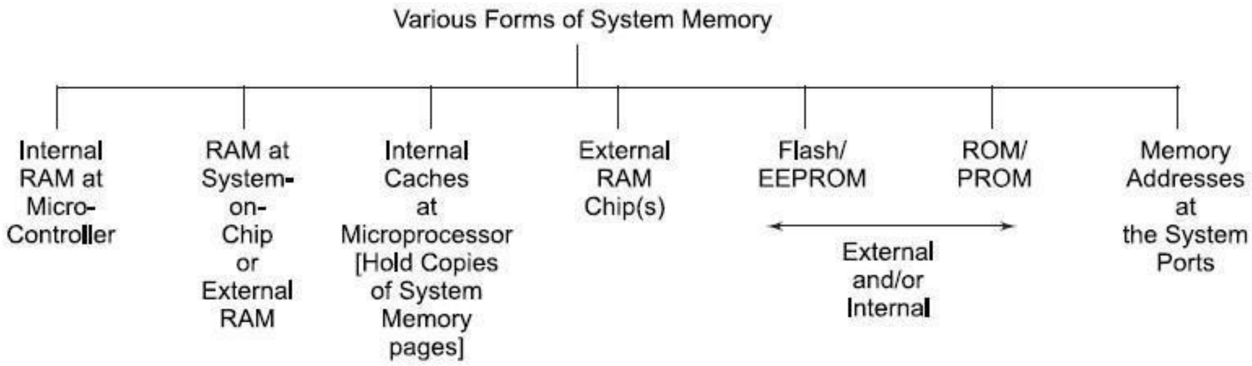
2.1 Memory and I/O Devices Interfacing:

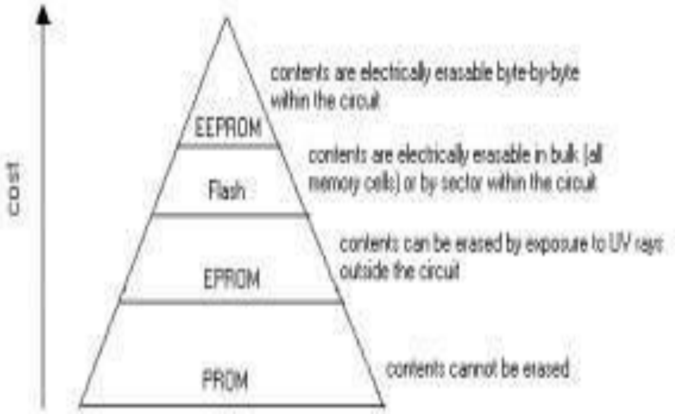
In a system, there are various types of memories.

1. Internal RAM
2. Internal ROM/PROM/EPROM
3. External RAM for the temporary data and stack
4. Internal caches
5. EEPROM or flash
6. External ROM or PROM for embedding software
7. RAM Memory buffers at the ports


Various Forms of System Memory
Internal RAM at Micro-Controller
RAM at System-on-Chip or External RAM
Internal Caches at Microprocessor [Hold Copies of System Memory pages]
External RAM Chip(s)
Flash/ EEPROM
ROM/ PROM
External and/or Internal
Memory Addresses at the System Ports

- The memory unit in an embedded system should have low access time and high density (a memory chip has greater density if it can store more bits in the same amount of space).
- Memory in an embedded system consists of ROM (only read operations permitted) and RAM (read and write operations are permitted).
- The contents of ROM are non-volatile (power failure does not erase the contents) while RAM is volatile.
- ROM stores the program code while RAM is used to store transient input or output data. Embedded systems generally do not possess secondary storage devices such as magnetic disks.

- As programs of embedded systems are small there is no need for virtual storage.


cost
EEPROM
contents are electrically erasable byte-by-byte within the circuit
Flash
contents are electrically erasable in bulk (all memory cells) or by sector within the circuit
EPROM
contents can be erased by exposure to UV rays outside the circuit
PROM
contents cannot be erased

Volatile memory:

❑ A primary distinction in memory types is volatility. Volatile memories only hold their contents while power is applied to the memory device.

❑ As soon as power is removed, the memories lose their contents; consequently, volatile memories are unacceptable if data must be retained when the memory is switched off.

❑ Examples of volatile memories include static RAM (SRAM),synchronous staticRAM (SSRAM), synchronous dynamic RAM (SDRAM), and FPGA on-chip memory.

Nonvolatile memory:

Non-volatile memories retain their contents when power is switched off,making them good choices for storing information that must be retrievedafter a system power-cycle. Processor boot-code, persistent application settings, and FPGA configuration data are typically stored in non- volatile memory.

Although non-volatile memory has the advantage of retaining its data when power is removed, it is typically much slower to write to than volatile memory, and often has more complex writing and erasing procedures.

Non-volatile memory is also usually only guaranteed to be erasable a given number of times, after which it may fail. Examples of non- volatile memories include all types of flash, EPROM, and EEPROM.

ROM Overview:

❑ Although there are exceptions, the ROM is generally viewed as read only device.when the ROM is implemented,positions in the array that are to storea logical 0 have a transistor connected as shown in figure. Those positions intended to store a logical 1 have none.

Static RAM overview:

❑ A high level interface to the SRAM is very similar to that for the ROM. The major differences arise from support for write capability. Figure 3.4 represents the major I/O signals and a typical cell in an SRAM array.

SDRAM:

SDRAM is another type of volatile memory. It is similar to SRAM, except that it is dynamic and must be refreshed periodically to maintain its content.

The dynamic memory cells in SDRAM are much smaller than the staticmemory cells used in SRAM.

This difference in size translates into very high-capacity and low-cost memory devices.

In addition to the refresh requirement, SDRAM has other very specific interface requirements which typically necessitate the use of special controller hardware.

Unlike SRAM, which has a static set of address lines, SDRAM divides up itsmemory space into banks, rows, and columns.

Switching between banks and rows incurs some overhead, so that efficientuse of SDRAM involves the careful ordering of accesses.

SDRAM also multiplexes the row and column addresses over the same address lines, which reduces the pin count necessary to implement a given size of SDRAM.

Higher speed varieties of SDRAM such as DDR, DDR2, and DDR3 also havestrict signal integrity requirements which need to be carefully considered during the design of the PCB.

SDRAM devices are among the least expensive and largest-capacity types of RAM devices available, making them one of the most popular.

Dynamic RAM Overview

❑ Larger microcomputer systems use Dynamic RAM (DRAM) rather than Static RAM (SRAM) because of its lower cost per bit.

❑ DRAMs require more complex interface circuitry because of their multiplexedaddress bus and because of the need to refresh each memory cell periodically.

❑ A typical DRAM memory is laid out as a square array of memory cells with anequal number of rows and columns.

❑ Each memory cell stores one bit. The bits are addressed by using half of the bits (the most significant half) to select a row and the other half to select a column.

❑ Each DRAM memory cell is very simple – it consists of a capacitor and a MOSFET switch. A DRAM memory cell is therefore much smaller than an SRAM cell which needs at least two gates to implement a flip-flop.

❑ The Input / output organization of a computer depends upon the size of computer and the peripherals connected to it. The I/O Subsystem of the computer, provides an efficient mode of communication between the centralsystem and the outside environment.

The most common input output devices are:
Monitor
Keyboard
Mouse
Printer
Magnetic tapes

❑ The devices that are under the direct control of the computer are said to be connected online.
Input Output Interface provides a method for transferring information between internal storage and external I/O devices. Peripherals connected to a computer need special communication links for interfacing them with the central processing unit. The purpose of communication link is to resolve thedifferences that exist between the central computer and each peripheral.

The Major Differences are:-

Peripherals are electromechnical and electromagnetic devices and CPU and memory areelectronic devices. Therefore, a conversion of signal values may be needed.
The data transfer rate of peripherals is usually slower than the transfer rate of CPU and consequently, a synchronization mechanism may be needed.
Data codes and formats in the peripherals differ from the word format in the CPU and memory.

The operating modes of peripherals are different from each other and must be controlled so as not to disturb the operation of other peripherals connected to the CPU.
To Resolve these differences, computer systems include special hardware components between the CPU and Peripherals to supervise and synchronizeall input and out transfers.
These components are called Interface Units because they interface between the processor bus and the peripheral devices.

I/O BUS and Interface Module It defines the typical link between the processor and several peripherals.

The I/O Bus consists of data lines, address lines and control lines. The I/Obus from the processor is attached to all peripherals interface.
To communicate with a particular device, the processor places a device address on address lines.

Each Interface decodes the address and control received from the I/O bus,interprets them for peripherals and provides signals for the peripheral controller.

It is also synchronizes the data flow and supervises the transfer betweenperipheral and processor.

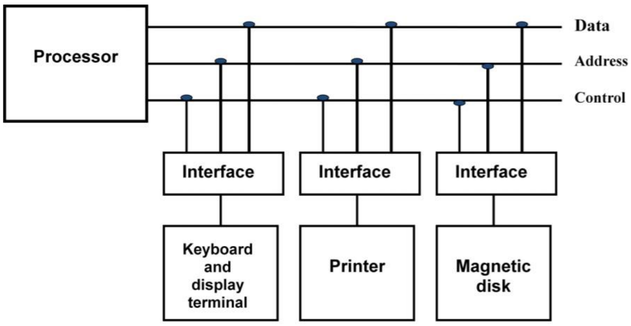
Each peripheral has its own controller. For example, the printer controller controls the paper motion, the print timing The control lines are referred as I/O command.

The commands are as following:

Control command- A control command is issued to activate the peripheraland to inform it what to do.

Status command- A status command is used to test various status conditionsin the interface and the peripheral.

Data Output command- A data output command causes the interface to respond by transferring data from the bus into one of its registers. Data Input command- The data input command is the opposite of the data output.



Connection of I/O bus to input-output devices

- To communicate with I/O, the processor must communicate with the memory unit. Like the I/O bus, the memory bus contains data, address andread/write control lines.
- There are 3 ways that computer buses can be used to communicate withmemory and I/O:
- Use two Separate buses, one for memory and other for I/O.
- Use one common bus for both memory and I/O but separate controllines for each.
- Use one common bus for memory and I/O with common control lines.
- I/O Processor In the first method, the computer has independent sets of data, address and control buses one for accessing memory and other for I/O. This is done in computers that provide a separate I/O processor (IOP).

The purpose of IOP is to provide an independent pathway for the transfer ofinformation between external device and internal memory.