Differential Amplifier

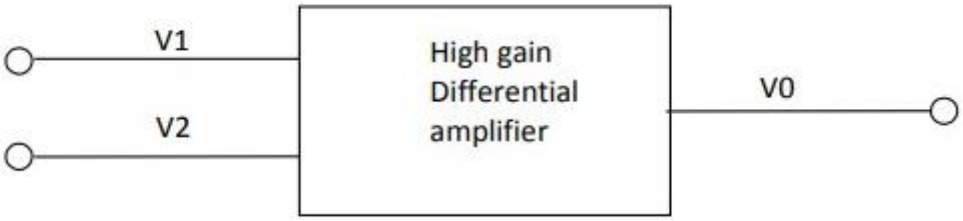
The function of a differential amplifier is to amplify the difference between two signals. The need for differential amplifier arises in many physical measurements where response from DC too many MHz of frequency is required. This forms the basic input stage of an integrated amplifier.

The basic differential amplifier has the following important properties of

- Excellent stability
- High versatility and
- High immunity to interference signals

The differential amplifier as a building block of the op-amp has the advantages of

- Lower cost
- Easier fabrication as IC component and
- closely matched components.



Block diagram of Differential amplifier

The above figure shows the basic block diagram of a differential amplifier, with two input terminals and one output terminal. The output signal of the differential amplifier is proportional to the difference between the two input signals.

$V_0 = A_{dm} (V_1 – V_2)$

If $V_1 = V_2$, then the output voltage is zero. A non-zero output voltage V0 is obtained when V_1 and V_2 are not equal. The difference mode input voltage is defined as $V_m = V_1 – V_2$ and the common mode input voltage is defined as

$$V_{CM}=\frac{V1+V2}{2}$$

These equation show that if $V_1 = V_2$, then the differential mode input signal is zero and common mode input signal is $V_{cm} = V_1 = V_2$.

Differential Amplifier with Active load:

Differential amplifier is designed with active loads to increase the differential mode voltage gain. The open circuit voltage gain of an op-amp is needed to be as large as possible. This is got by cascading the gain stages which increase the phase shift and the amplifier also becomes vulnerable to oscillations. The gain can be increased by using large values of collector resistance. For such a circuit, the voltage gain is given by

A_{dm} = gm RC

To increase the gain the IC RC product must be made very large. However, there are limitations in IC fabrication such as,

1. A large value of resistance needs a large chip area.
2. For large RC, the quiescent drop across the resistor increase and a large power supply will be required to maintain a given operating current.
3. Large monolithic resistor introduces large parasitic capacitances which limits the frequency response of the amplifier.
4. for linear operation of the differential pair, the devices should not be allowed to enter into saturation. This limits the max input voltage that can be applied to the bases of transistors Q_1 and Q_2 the base-collector junction must be allowed to become forward-biased by more than 0.5V. The large value of load resistance produces a large dc voltage drop (I_{EE} / 2) R_C, so that the collector voltage will be V_C=Vcc - (IEE/2) RC and it will be substantially less than the supply voltage Vcc. This will reduce the input voltage range of the differential amplifier. Due to the reasons cited above, an active load is preferred in the differential amplifier configurations.

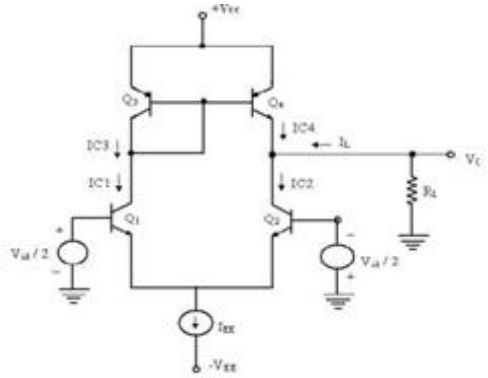
BJT Differential Amplifier using active loads:

A simple active load circuit for a differential amplifier is the current mirror active load as shown in figure. The active load comprises of transistors Q_3 and Q_4 with the transistor Q_3 connected as a Diode with its base and collector shorted. The circuit is shown to drive a load RL. When an ac input voltage is applied to the differential amplifier, the various currents of the circuit are given by $I_{C4} = I_{C3} = I_{C1}$ = gmVid/2 where $I_{C4} = I_{C3}$ due to current mirror action.

I_{C2} = - gmVid/2 .

We know that the load current IL entering the next stage is $I_L = I_{C2} - I_{C4}$ = - gmVid/2 - gmVid/2 = - gmVid

Then, the output voltage from the differential= amplifier= is given by $V_0 = - I_L R_L$ = gm $R_L V_{id}$. The ac voltage gain of the circuit is given by $A_v = v_0/v_{id}$ = gmR_L. The amplifier can amplify the differential input signals and it provides single-ended output with a ground reference since the load R_L is connected to only one output terminal. This is made possible by the use of the current mirror active load. The output resistance R0 of the circuit is that offered by the parallel combination of transistors Q_2 (NPN) and Q_4(PNP). It is given by $R_r = r_{02} \parallel r_{04}$.



BJT differential amplifier with current mirror active load

Analysis of BJT differential amplifier with active load:

The collector currents of all the transistors are equal.

$I_{C1} = I_{C2} = I_{C3} = I_{C4} = I_{EE}/2$.

The Collector -emitter voltages of Q_1 and Q_2 are given by

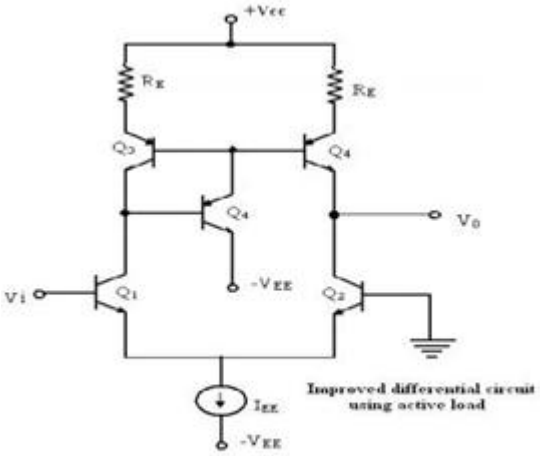
$V_{CE1}-V_{CE2} = V_C-V_E=V_{CC} - V_{EB}-(-V_{EB})= V_{CC}$

Eqn. shows that, the offset is higher than that of a resistive loaded differential amplifier A. This can be reduced by the use of emitter resistors for Q_3 and Q_4 , and a transistor Q_5in the current mirror load.

CMRR of the differential amplifier using active load:

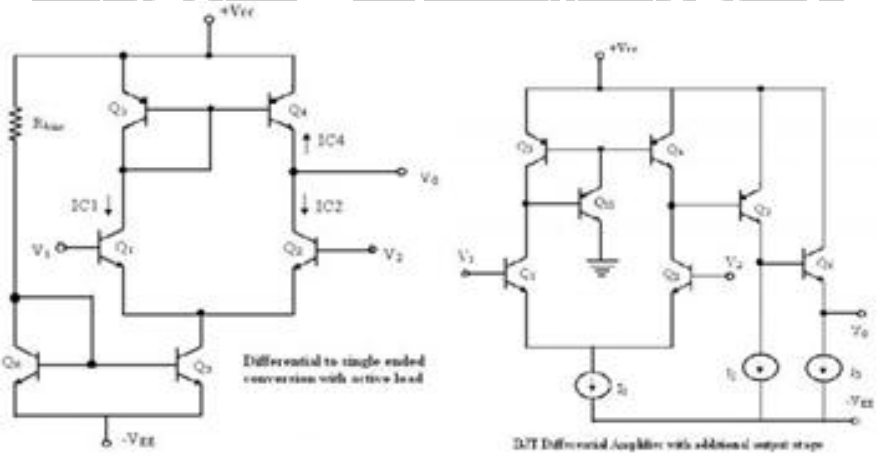
The differential amplifier using active load provides high voltage gain to the differential input signal and a single – ended output that is referenced to the ground is obtained. The differential amplifier which provides conversion for a differential signal to a single ended signal is necessary in differential input signal ended output amplifiers. The op-amp is one such circuit. The changes in the common-mode signal of the bias current source. This induces a change in I_{C2} and an identical change in I_{C1}. The change in I_{C1}will then produce a change in the PNP load devices, and thereby a change in I_{C4}, which is the collector current Q_4, The current I_{C4} is in such a direction as to cancel the change in I_{C2}. As a result of this, any common mode input does not cause a change in output.

The voltage gain of the differential amplifier is independent of the quiescent current I_{EE}. This makes it possible to use very small value of I_{EE} as low as 20μA, while still maintaining a large voltage gain. Small value of I_{EE} is preferred, since it results in a small value of bias current and a large value for the input resistance. A limitation in choosing a small I_{EE} is, however, the fact that, it will result in a poor frequency response of the amplifier.



Improved differential circuit using active load

When a small value of bias current is required, the best approach is to use a JFET or MOSFET differential amplifier that is operated at comparatively higher values of I_{EE}.



Differential to single ended conversion and output stage

Differential Mode signal analysis:

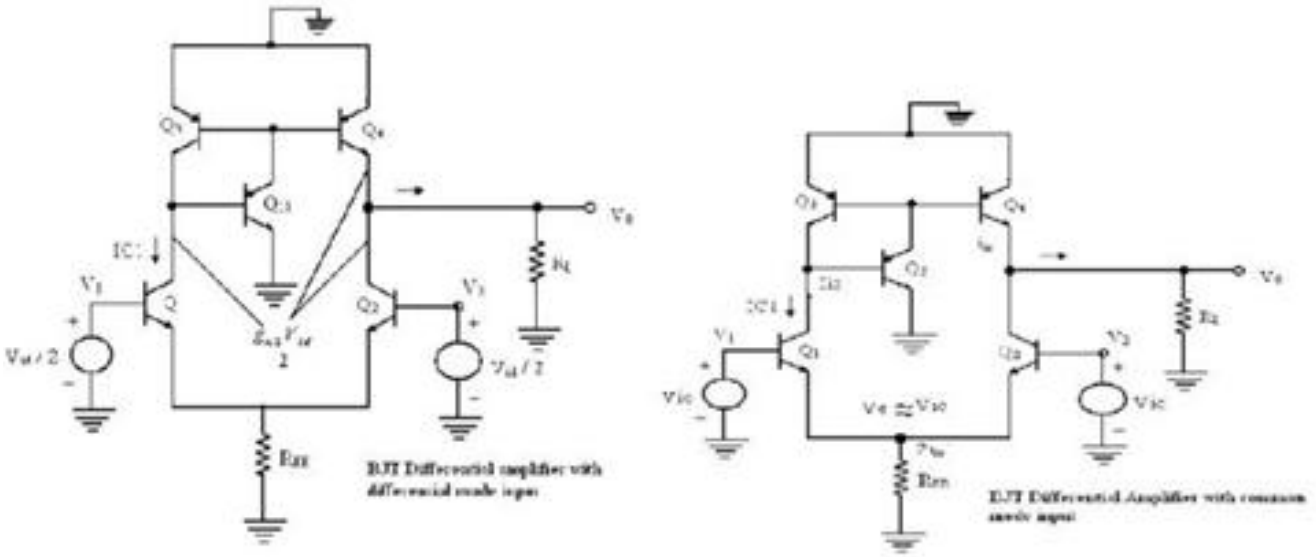
The ac analysis of the differential amplifier can be made using the circuit model as shown below. The differential input transistor pair produces equal and opposite currents whose amplitude us given by gm2 V_{id} /2 at the collector of Q_1 and Q_2. The collector current I_{c1} is fed by the transistor Q_3 and it is mirrored at the output of Q_4. Therefore, the total current i_0 flowing through the load resistor R_L is given by $i_0 = [2g_{m2}V_{id}]/2 = g_{m2}V_{id}$. Then the output voltage is $v_0 = i_0R_L - g_{m2}R_Lv_{id}$ and the differential mode gain Ad of the differential amplifier is

$$A_{dm} = \frac{v_0}{v_{dm}} = g_{m2}R_L$$

This current mirror provides a single ended output which has a voltage equal to the maximum gain of the common emitter amplifier.

The power of the current mirror can be increased by including additional common collector stages at the o/p of the differential input stage. A bipolar differential amplifier structure with additional stages is shown in figure. The resistance at the output of the differential stage is now given by the parallel combination of transistors Q_2 and Q_4 and the input resistance is offered by Q_5. Then, the equivalent resistance is expressed by $Req = r_{o2} \parallel r_{04} \parallel r_{i5} = r_{i5}$.

The gain of the differential stage then becomes $Adm = g_{m2} R_{eq} = g_{m2} r_{i5} = \beta I_{C2}/I_{C5}$.



Differentail amplifier with differential mode input and common mode input