WRITTING TESTBENCHES IN VERILOG HDL

- Only clocked D-type master-slave flip-flops for all state variables should be used.
- At least one PI pin must be available for test. It is better if more pins are available.
- All clock inputs to flip-flops must be controlled from primary inputs (PIs). There will be no gated clock. This is necessary for FFs to function as a scan register.
- Clocks must not feed data inputs of flip-flops. A violation of this can lead to a race condition in the normal mode.

Scan Overheads

The use of scan design produces two types of overheads. These are area overhead and performance overhead. The scan hardware requires extra area and slows down the signals.

- **IO pin overhead:** At least one primary pin necessary for test.
- **Area overhead:** *Gate overhead* = [4 $n_{SFF}/(n_G+10n_{FF})$] x 100%, where n_G = number of combinational gates; n_{FF} = number of flip-flops; n_{SFF} = number of scan flip-flops; For full scan number of scan flip-flops is equal to the number of original circuit flip-flops. Example: n_G = 100k gates, n_{FF} = 2k flip-flops, overhead = 6.7%. For more accurate estimation scan wiring and layout area must be taken into consideration.
- **Performance overhead:** The multiplexer of the scan flip-flop adds two gate-delays in combinational path. Fanouts of the flip-flops also increased by 1, which can increase the clock period.

Testbench Variations

There have been many variations of scan as listed below, few of these are discussed here.

- MUXed Scan
- Scan path
- Scan-Hold Flip-Flop
- Serial scan
- Level-Sensitive Scan Design (LSSD)
- Scan set
- Random access scan

- It was invented at Stanford in 1973 by M. Williams & Angell.
- In this approach a MUX is inserted in front of each FF to be placed in the scan chain.
- operation mode and when T=1, it is in test mode (or shift-register mode).
- The scan flip-flips (FFs) must be interconnected in a particular way. This approach effectively turns the sequential testing problem into a combinational one and can be fully tested by compact ATPG patterns.
- There are two types of overheads associated with this method. The hardware overhead due to three extra pins, multiplexers for all FFs, and extra routing area. The performance overhead includes multiplexer delay and FF delay due to extra load.

- This approach is also called the Clock Scan Approach.
- It was invented by Kobayashi *et al.* in 1968, and reported by Funatsu *et al.* in 1975, and adopted by NEC.
- In this approach multiplexing is done by two different clocks instead of a MUX.

- It uses two-port raceless D-FFs as shown in Figure 39.3. Each FF consists of two latches operating in a master-slave fashion, and has two clocks (C1 and C2) to control the scan input (SI) and the normal data input (DI) separately.
- The two-port raceless D-FF is controlled in the following way:
- For normal mode operation C2 = 1 to block SI and C1 = 0 →1 to load DI.
- For shift register test mode C1 = 1 to block DI and C2 = 0 →1 to load SI.
- This approach gives a lower hardware overhead (due to dense layout) and less performance penalty (due to the removal of the MUX in front of the FF) compared to the MUX Scan Approach. The real figures however depend on the circuit style and technology selected, and on the physical implementation.

Scan-Based Techniques

The controllability and observability can be enhanced by providing more accessible logic nodes with use of additional primary input lines and multiplexors.However, the use of additional I/O pins can be costly not only for chip fabrication but also for packaging. A popular alternative is to use scan registers with both shift and parallel load capabilities. The scan design technique is a structured approach to design sequential circuits for testability.

The storage cells in registers are used as observation points, control points, or both. By using the scan design techniques, the testing of a sequential circuit is reduced to the problem of testing a combinational circuit.In general, a sequential circuit consists of a combinational circuit and some storage elements. In the scan-based design, the storage elements are connected to form a long serial shift register, the so-called scan path, by using multiplexors and a mode (test/ normal) control signal, as shown in Fig. 1 .In the test mode, the scan-in signal is clocked into the scan path, and the output of the last stage latch is scanned out. In the normal mode, the scan-in path is disabled and the circuit functions as a sequential circuit. The testing sequence is as follows:

Step 1: Set the mode to test and, let latches accept data from scan-in input.
Step 2: Verify the scan path by shifting in and out the test data.

Step 3: Scan in (shift in) the desired state vector into the shift register.
Step 4: Apply the test pattern to the prim ary input pins.
Step 5: Set the mode to normal and observe the primary outputs of the circuit after sufficient time for propagation.,
Step 6: Assert the circuit clock, for one machine cycle to capture the outputs of the combinational logic into the registers.
Step 7: Return to test mode; scan out the contents of the registers, and at the same time scan in the next pattern.
Step 8: Repeat steps 3-7 until all test patterns are applied.