2.4 ADC TYPES

FLASH TYPE ADC

Flash type ADC produces an equivalent digital output for a corresponding analog input in no time. Hence, flash type ADC is the fastest ADC.The circuit diagram of a 3-bit flash type ADC is shown in the following figure 4.6.1.

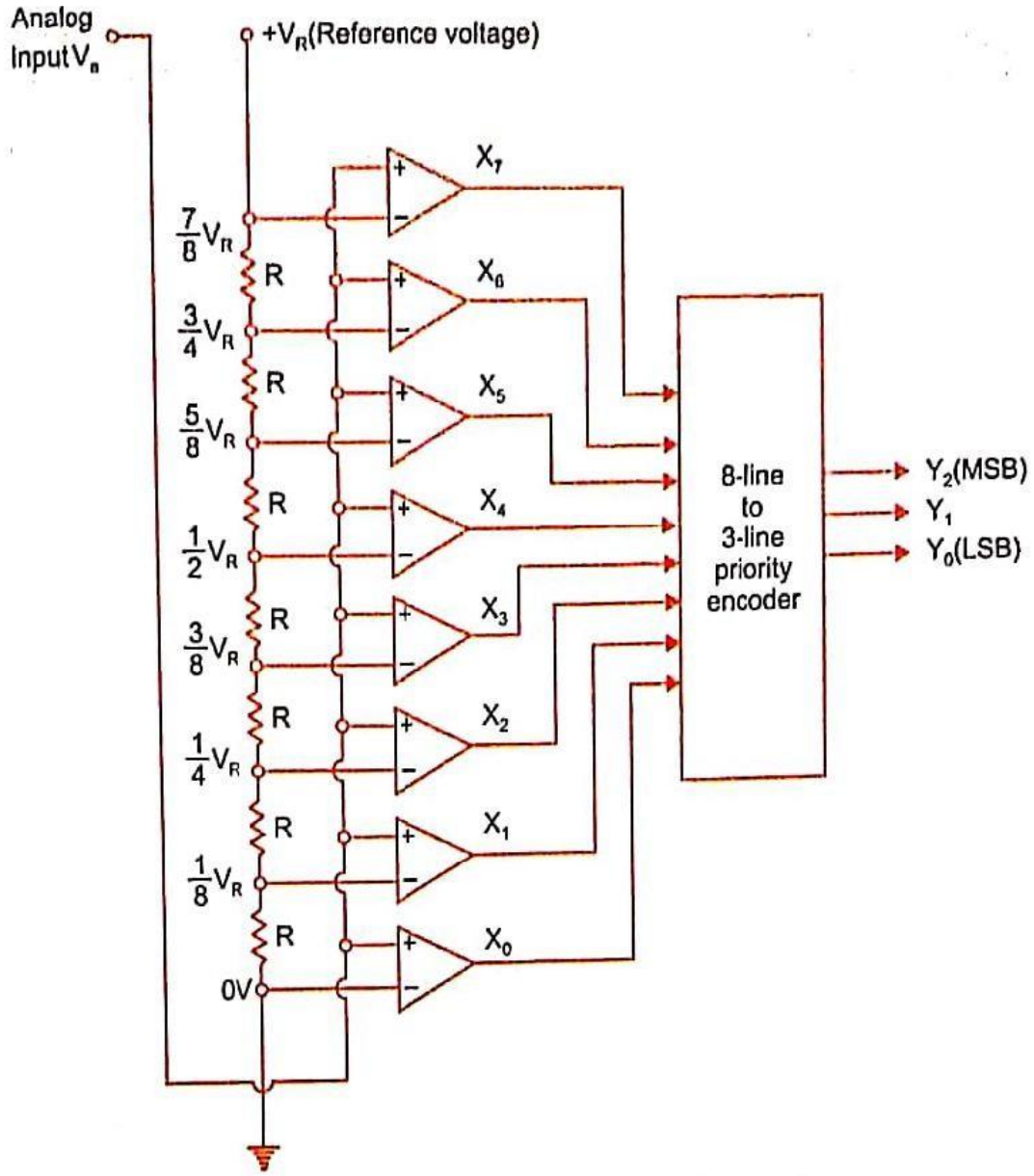

Figure 4.6.1.Basic circuit for flash type A/D converter

[source:"Linear Integrated Circuits"by D.Roy Choudhry, Shail Bala Jain, Page-413]

The 3-bit flash type ADC consists of a voltage divider network, 7 comparators and a priority encoder.

The **working** of a 3-bit flash type ADC is as follows.

- The **voltage divider network** contains 8 equal resistors. A reference voltage VR is applied across that entire network with respect to the ground. The voltage drop across each resistor from bottom to top with respect to ground will be the integer multiples (from 1 to 8) of VR8VR8.
- The external **input voltage** Vi is applied to the non-inverting terminal of all comparators. The voltage drop across each resistor from bottom to top with respect to ground is applied to the inverting terminal of comparators from bottom to top.
- At a time, all the comparators compare the external input voltage with the voltage drops present at the respective other input terminal. That means, the comparison operations take place by each comparator **parallelly**.
- The **output of the comparator** will be '1' as long as Vi is greater than the voltage drop present at the respective other input terminal. Similarly, the output of comparator will be '0', when, Vi is less than or equal to the voltage drop present at the respective other input terminal.
- All the outputs of comparators are connected as the inputs of **priority encoder**.This priority encoder produces a binary code (digital output), which is corresponding to the high priority input that has '1'.
- Therefore, the output of priority encoder is nothing but the binary equivalent **(digital output)** of external analog input voltage, Vi.

The flash type ADC is used in the applications where the conversion speed of analog input into digital data should be very high.

SUCCESSIVE APPROXIMATION TYPE ADC

Successive Approximation type ADC is the most widely used and popular ADC method. The conversion time is maintained constant in successive approximation type ADC, and is proportional to the number of bits in the digital output, unlike the counter and continuous type A/D converters. The basic principle of this type of A/D converter is that the unknown analog input voltage is approximated against an n-bit digital value by trying one bit at a time,

beginning with the MSB. The principle of successive approximation process for a 4-bit conversion is explained here. This type of ADC operates by successively dividing the voltage range by half, as explained in the following steps.

(1) The MSB is initially set to 1 with the remaining three bits set as 000. The digital equivalent voltage is compared with the unknown analog input voltage.

(2) If the analog input voltage is higher than the digital equivalent voltage, the MSB is retained as 1 and the second MSB is set to 1. Otherwise, the MSB is set to 0 and the second MSB is set to 1. Comparison is made as given in step (1) to decide whether to retain or reset the second MSB.

The above steps are more accurately illustrated with the help of an example. Let us assume that the 4-bit ADC is used and the analog input voltage is V_A = 11 V. when the conversion starts, the MSB bit is set to 1.

Now $V_A = 11V > V_D = 8V = [1000]2$.Since the unknown analog input voltage VA is higher than the equivalent digital voltage VD, as discussed in step (2), the MSB is retained as 1 and the next MSB bit is set to 1 as follows

$V_D = 12V = [1100]2$

Now $V_A = 11V < V_D = 12V = [1100]2$.Here now, the unknown analog input voltage VA is lower than the equivalent digital voltage V_D. As discussed in step (2), the second MSB is set to 0 and next MSB set to 1 as $V_D = 10V = [1010]2$

Now again $V_A = 11V > V_D = 10V = [1010]2$.Again as discussed in step (2) $V_A > V_D$, hence the third MSB is retained to 1 and the last bit is set to 1. The new code word is $V_D = 11V = [1011]2$.Now finally $V_A = V_D$, and the conversion stops. The functional block diagram of successive approximation type of ADC is shown in figure 4.6.2 below.

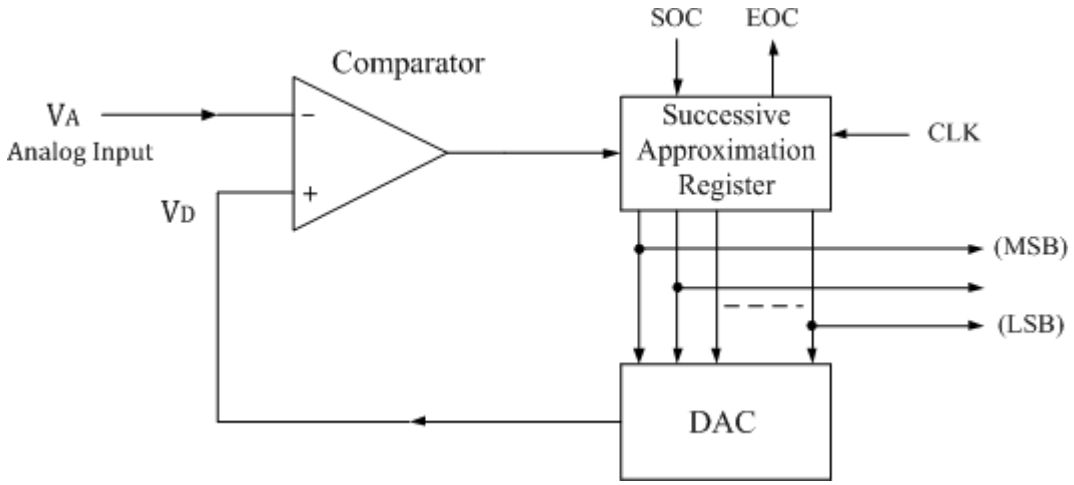

Figure 4.6.2 Functional diagram of successive approximation type of ADC

[https://www.electronics-tutorial.net/analog-integrated-circuits/data-converters/successive-approximation-type-adc/]

It consists of a successive approximation register (SAR), DAC and comparator. The output of SAR is given to n-bit DAC. The equivalent analog output voltage of DAC, VD is applied to the non-inverting input of the comparator. The second input to the comparator is the unknown analog input voltage VA. The output of the comparator is used to activate the successive approximation logic of SAR.When the start command is applied, the SAR sets the MSB to logic 1 and other bits are made logic 0, so that the trial code becomes 1000.

Advantages:

1.Conversion time is very small.

2. Conversion time is constant and independent of the amplitude of the analog input signal VA.

Disadvantages:

1.Circuit is complex.

2. The conversion time is more compared to flash type ADC.

SINGLE SLOPE ADC

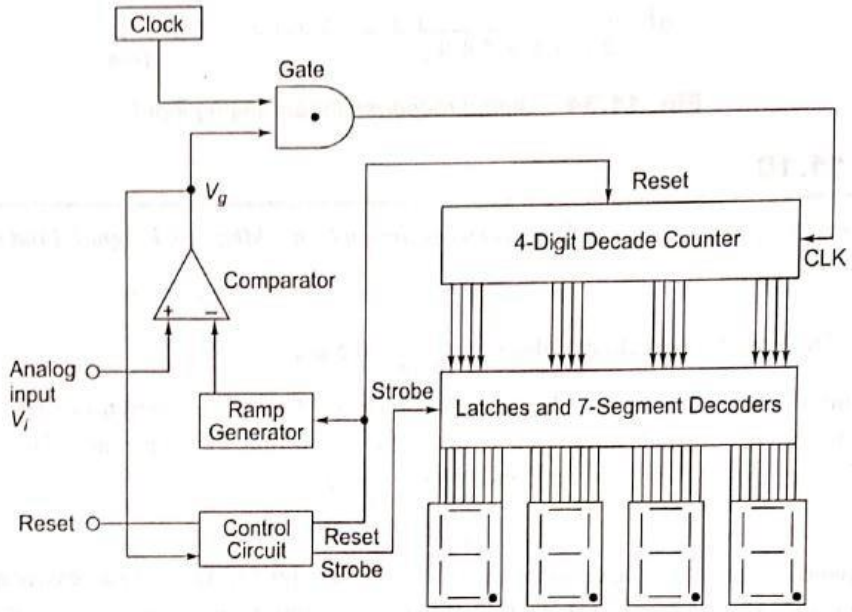

Figure 4.6.3.Block Diagram of single slope ADC

[source:"Linear Integrated Circuits"by S.Salivahanan& V.S. Kanchana Bhaskaran, Page-488]

Figure 4.6.3 shown above is the block diagram of single slope ADC.These converter techniques are based on comparing the unknown analog i/p voltage with a reference voltage that begins at 0v & increases linearly with time.The time required for the reference voltage to reach the value of unknown analog i/p voltage is proportional to the amplitude of unknown analog i/p voltage.The time period can be measured using a digital counter.The main circuit of this converter is a ramp generator which on receiving a RESET from the control circuit increases linearly with time from 0v to a max volt Vm Assume a +ive analog i/p voltage Vi is applied at the non-inverting i/p of the comparator.When a RESET signal is applied to the control logic, the 4-digit decade counter resets to 0 & the ramp begins to increase.Vi is +ive the comparator o/p is in HIGH state.

This allows the clk pulse to pass to the i/p of the 4-digit counter through the AND gate & the counter is incremented.This process continues until the analog i/p voltage is greater than the ramp generator voltage.When the ramp generator voltage is equal to the analog i/p voltage, the comparator o/p becomes negatively saturated or logic 0.The clk is prevented from passing through the gate causing the counter operation.Then the control circuit generates a STROBE

signal,which latches the counter values in the 4-digit latch,which is displayed on 7-segmant displays.The displayed value is then equivalent to the amplitude of analog input voltage.

DUAL SLOPE ADC

The analog part of the circuit consists of a high input impedance buffer A_1, precision integrator A_2 and a voltage comparator.The converter first integrates the analog input signal V_a for a fixed duration of 2^n clk periods.Then it integrates an internal reference voltage V_R of opposite polarity until the integrator output is zero. Functional diagram of the dual slope ADC and Integrated output waveform for the dual slope ADC is shown in figure 4.6.4 a) and b).

Before the START command arrives,the switch SW_1 is connected to ground and SW_2 is closed.Any offset voltage present in the A_1,A_2,comparator loop after integration appears across the capacitor CAZ till the threshold of the comparator is achieved.The capacitor CAZ thus provides automatic compensation for the input-offset voltages of all the three amplifiers.

Later when SW2 opens,CAZ acts as a memory to hold the voltages required to keep the offset nulled. At the arrival of the START command at t=t1,the control logic opens SW_2 and connects to V_a and enables the counter starting from zero.The circuit uses an n-stage ripple counter and therefore the counter resets to zero after counting 2^n pulses.The analog voltage V_a is integrated for a fixed number 2^n counts of clk pulses after which the counter resets to zero.If the clock period is T the integration take place for a time $T=2^n$ x T and the output is a ramp going downwards.

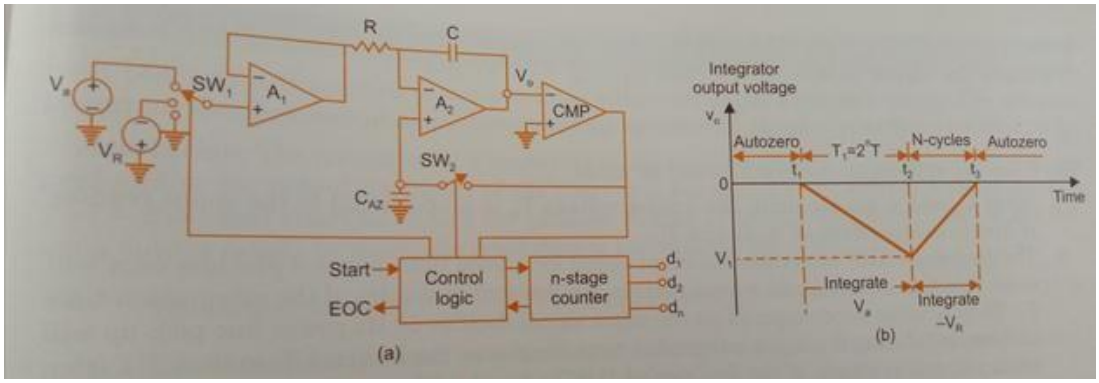

Figure 4.6.4.a) Functional diagram of the dual slope ADC b)Integrated output waveform for the dual slope ADC

[source:"Linear Integrated Circuits"by D.Roy Choudhry, Shail Bala Jain, Page-419]

The counter resets itself to zero at the end of the integral T_1 and the switch SW_1 is connected to the reference voltage $-V_R$. The output voltage Vo will now have a +ive slope.As long as V_o is –ive ,the output of the comparator is +ive and the control logic allows the clock pulse to be counted.When Vo become just zero at time $t=t_3$,the control logic issues an end of conversion(EOC) command and no further clock pulses enter the counter.

$$T_1 = t_2 - t_1 = \frac{2^n counts}{clock\ rate}$$

$$t_3 - t_2 = \frac{digital\ count\ N}{clock\ rate}$$

$$For\ an\ integrator, \Delta V_o = (-{}^{1}/_{RC})V(\Delta t)$$

Voltage Vo will be equal to V1 at the instant t2 and can be given as

$$V_1 = (-{}^{1}/_{RC})V_a(t_2 - t_1)$$

The voltage V1 is also given by

$$V_1 = (-{}^{1}/_{RC})(-V_R)(t_2 - t_3)$$

$$so, V_a(t_2 - t_1) = V_R(t_3 - t_2)$$

$$sub\ t_2 - t_1 = 2^n\ \&\ t_3 - t_2 = N$$

$$V_a(2^n) = V_R(N)$$

$$V_a = V_R({}^{N}/_{2^n})$$