DC Characteristics of op-amp

Current is taken from the source into the op-amp inputs respond differently to current and voltage due to mismatch in transistor.

DC output voltages are,

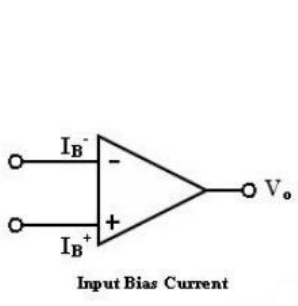
- Input bias current
- Input offset current
- Input offset voltage
- Thermal drift

Input bias current:

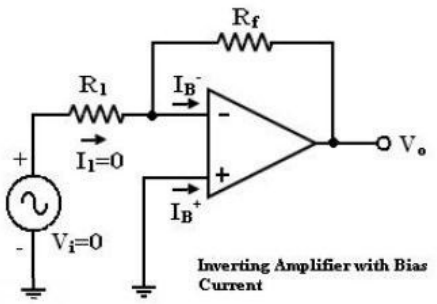
The op-amp‘s input is differential amplifier, which may be made of BJT or FET.

In an ideal op-amp, we assumed that no current is drawn from the input terminals the base currents entering into the inverting and non-inverting terminals (I_B^- & I_B^+ respectively).

Even though both the transistors are identical, I_B^- and I_B^+ are not exactly equal due to internal imbalance between the two inputs. Manufacturers specify the input bias current I_B



Input Bias Current



Inverting Amplifier with Bias Current

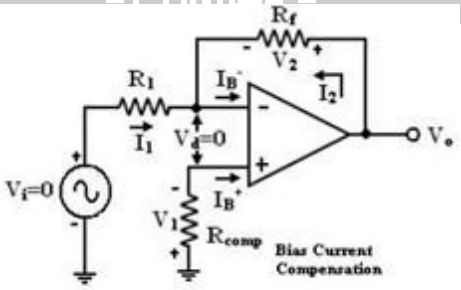
$$I_B = \frac{I_B^+ + I_B^-}{2}$$

If input voltage $V_i = 0V$. The output Voltage Vo should also be ($V_o = 0$) but for $I_B = 500nA$ We find that the output voltage is offset by Op-amp with a 1M feedback resistor

Vo = 500nA X 1M = 500mV

The output is driven to 500mV with zero input, because of the bias currents.

In application where the signal levels are measured in mV, this is totally unacceptable. This can be compensated by a compensation resistor R_{comp} has been added between the non-inverting input terminal and ground as shown in the figure below.



Bias compensated circuit

Current I_B^+ flowing through the compensating resistor R_{comp}, then by KVL we get,

$-V_1+0+V_2-V_o = 0$ (or)

$V_o = V_2 - V_1$----------(1)

By selecting proper value of R_{comp}, V_2 can be cancelled with V_1 and the $V_o = 0$. The value of Rcomp is derived as

$V_1 = I_B^+ R_{comp}$ (or)

$I_B^+ = V_1/R_{comp}$ ----------(2)

The node 'a' is at voltage ($-V_1$). Because the voltage at the non-inverting input terminal is ($-V_1$).

So with $V_i = 0$ we get,

$I_1 = V_1/R_1$ ----------(3)

$I_2 = V_2/R_f$ (4)

For compensation, V_o should equal to zero ($V_o = 0$, $V_i = 0$). i.e. from equation (3) $V_2 = V_1$. So that,

$I_2 = V_1/R_f$ ——> (5)

KCL at node 'a' gives,

$I_B^- = I_2 + I_1 = (V_1/R_f) + (V_1/R_1) = V_1(R_1+R_f)/R_1R_f$ ----------(5)

Assume $I_B^- = I_B^+$ and using equation (2) & (5) we get

$V_1 (R_1+R_f)/R_1R_f = V_1/R_{comp}$

$R_{comp} = R_1 \parallel R_f$ ---------- (6)

i.e. to compensate for bias current, the compensating resistor, Rcomp should be equal to the parallel combination of resistor R_1 and R_f.

Input offset current:

i. Bias current compensation will work if both bias currents I_B^+ and I_B^- are equal.

ii. Since the input transistor cannot be made identical. There will always be some small difference between I_B^+ and I_B^-. This difference is called the offset current

$|Ios| = I_B^+ - I_B^-$ ----------(7)

Offset current I_{os} for BJT op-amp is 200nA and for FET op-amp is 10pA. Even with bias current compensation, offset current will produce an output voltage when $V_i = 0$.

$V_1 = I_B^+ R_{comp}$ ---------- (11)

And $I_1 = V_1/R_1$ ---------- (12)

KCL at node a gives,

$$I_2 = (I_B^- - I_1) = I_B^- - (I_B^+ \frac{R_{comp}}{R_1})$$

Output voltage □□ = □□□

Again $V_0 = I_2 R_f - V_1$

$Vo = I_2 R_f - I_B^+ R_{comp}$

$Vo = 1M\ \Omega \times 200nA$

$Vo = 200mV$ with $V_i = 0$

Equation (16) the offset current can be minimized by keeping feedback resistance small.

- Unfortunately to obtain high input impedance, R1 must be kept large.
- R1 large, the feedback resistor Rf must also be high. So as to obtain reasonable gain.

The T-feedback network is a good solution. This will allow large feedback resistance, while keeping the resistance to ground low (in dotted line).

The T-network provides a feedback signal as if the network were a single feedback resistor.

By T to Π conversion,

$$R_f = \frac{R_t^2 + 2R_tR_s}{R_s}$$

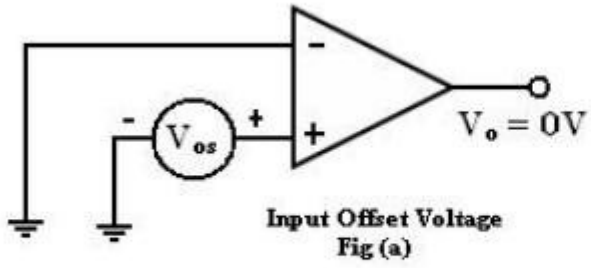
To design T- network first pick Rt<<Rf/2 and=calculate

$$R_s = \frac{R_t^2}{R_f - 2R_t}$$

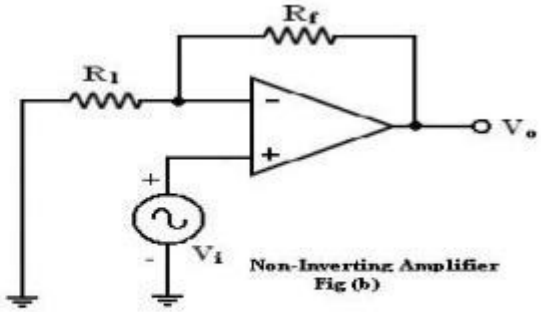
Input offset voltage:

In spite of the use of the above compensating techniques, it is found that the output voltage may still not be zero with zero input voltage [Vo ≠ 0 with Vi= 0]. This is due to unavoidable imbalances inside the op-amp and one may have to apply a small voltage at the input terminal to make output (Vo) = 0.

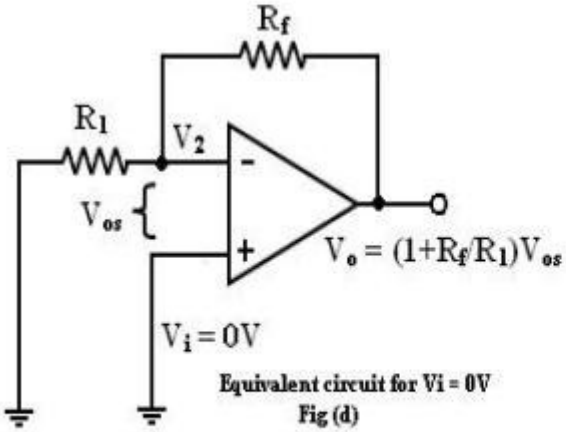
This voltage is called input offset voltage Vos. This is the voltage required to be applied at the input for making output voltage to zero (Vo = 0).



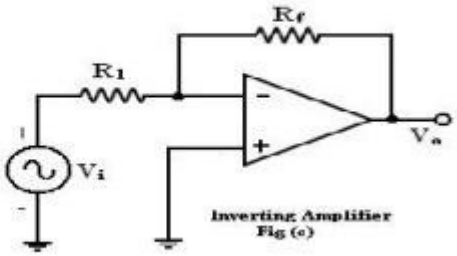
Input Offset Voltage
Fig (a)



Non-Inverting Amplifier
Fig (b)



Equivalent circuit for Vi = 0V
Fig (d)

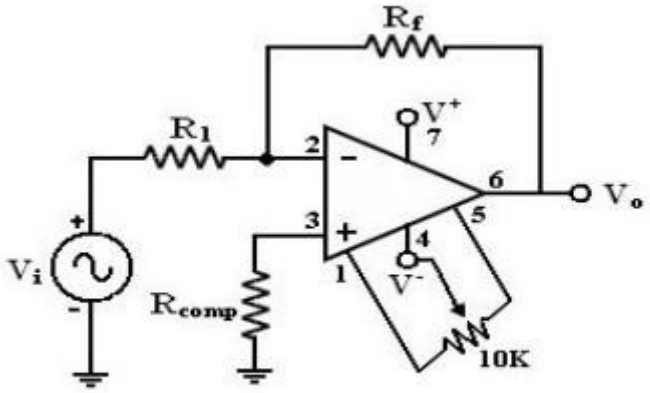


Inverting Amplifier
Fig (c)

Let us determine the Vos on the output of inverting and non-inverting amplifier. If $V_i = 0$ (Fig (b) and (c)) become the same as in figure (d).

Total output offset voltage:

The total output offset voltage V_{OT} could be either more or less than the offset voltage produced at the output due to input bias current (I_B) or input offset voltage alone(V_{os}). This is because IB and Vos could be either positive or negative with respect to ground. Therefore the maximum offset voltage at the output of an inverting and non-inverting amplifier (figure b, c) without any compensation technique used is given by many op amps provide offset compensation pins to nullify the offset voltage. A 10K potentiometer is placed across offset null pins 1&5. The wipes connected to the negative supply at pin 4. The position of the wipes is adjusted to nullify the offset voltage.



Compensation circuit for offset voltage

When the given (below) op-amps does not have these offset null pins, external balancing techniques are used.

$$V_{OT} = \left(1 + \frac{R_f}{R_1}\right) V_{OS} + R_f I_B$$

With Rcomp, the total output offset

$$V_{OT} = \left(1 + \frac{R_f}{R_1}\right) V_{OS} + R_f I_{OS}$$

Thermal drift:

Bias current, offset current, and offset voltage change with temperature. A circuit carefully nulled at 25ºC may not remain. So when the temperature rises to 35ºC. This is called drift. Offset current drift is expressed in nA/ºC. These indicate the change in offset for each degree Celsius change in temperature.