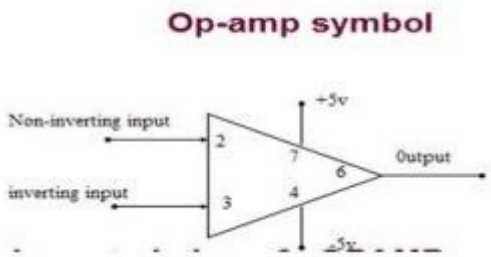
Basic information about operational amplifiers

An operational amplifier is a direct coupled high gain amplifier consisting of one or more differential amplifiers, followed by a level translator and an output stage.
It is a versatile device that can be used to amplify ac as well as dc input signals & designed for computing mathematical functions such as addition, subtraction ,multiplication, integration & differentiation.

Ideal operational Amplifiers
Infinite input resistance Ri, so that almost any signal source can drive it and there is no loading of the proceeding stage.

Ideal operational Amplifiers



Ideal op-amp characteristics:

- Infinite voltage gain A.
- Infinite input resistance Ri, so that almost any signal source can drive it and there is no loading of the proceeding stage.
- Zero output resistance Ro, so that the output can drive an infinite number of other devices.
- Zero output voltage, when input voltage is zero.
- Infinite bandwidth, so that any frequency signals from o to ∞ HZ can be amplified with out attenuation.
- Infinite common mode rejection ratio, so that the output common mode noise voltage is zero.
- Infinite slew rate, so that output voltage changes occur simultaneously with input voltage changes.

General Operational Amplifier stages and internal circuit diagrams of IC 741
An operational amplifier generally consists of three stages, namely 1. A differential amplifier 2. Additional amplifier stages to provide the required voltage gain and dc level shifting. 3. An emitter-follower or source follower output stage to provide current gain and low output resistance.

General Operational Amplifier stages and internal circuit diagrams of IC 741
An operational amplifier generally consists of three stages, namely

1. A differential amplifier
2. Additional amplifier stages to provide the required voltage gain and dc level shifting.
3. An emitter-follower or source follower output stage to provide current gain and low output resistance.

A low-frequency or dc gain of approximately 104 is desired for a general purpose op-amp and hence, the use of active load is preferred in the internal circuitry of op-amp.
The output voltage is required to be at ground, when the differential input voltages are zero, and this necessitates the use of dual polarity supply voltage. Since the output resistance of op-amp is required to be low, a complementary push-pull emitter – follower or source follower output stage is employed. Moreover, as the input bias currents are to be very small of the order of pico amperes, an FET input stage is normally preferred.

Input stage:

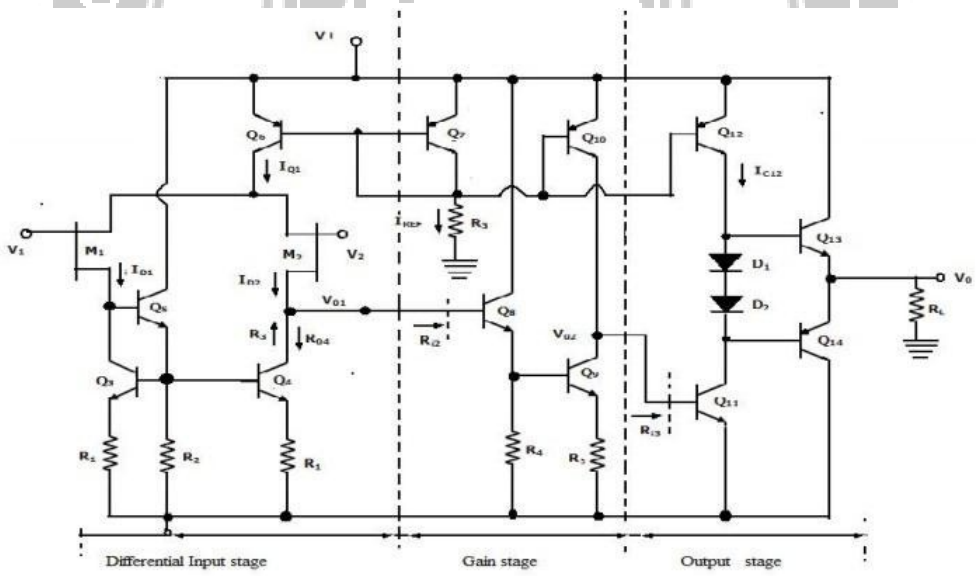
The input differential amplifier stage uses p-channel JFETs M_1 and M_2. It employs a three-transistor active load formed by Q_3, Q_4, and Q_5. The bias current for the stage is provided by a two-transistor current source using PNP transistors Q_6 and Q_7. Resistor R_1increases the o utput resistance seen looking into the collector of Q_4 as indicated by R_{04}. This is necessary to provide bias current stability against the transistor parameter variations. Resistor R_2 establishes a definite bias current through Q_5. A single ended output is taken out at the collector of Q_4.

MOSFET‘s are used in place of JFETs with additional devices in the circuit to prevent any damage for the gate oxide due to electrostatic discharges.

Gain stage:

The second stage or the gain stage uses Darlington transistor pair formed by Q_8 and Q_9as shown in figure. The transistor Q8 is connected as an emitter follower, providing large input resistance.

Therefore, it minimizes the loading effect on the input differential amplifier stage. The transistor Q_9 provides an additional gain and Q_{10} acts as an active load for this stage. The current mirror formed by Q_7 and Q_{10} establishes the bias current for Q_9. The VBE drop across Q_9 and drop across R_5 constitute the voltage drop across R_4, and this voltage sets the current through Q_8. It can be set to a small value, such that the base current of Q_8also is very less.



Output stage:

The final stage of the op-amp is a class AB complementary push-pull output stage. Q_{11} is an emitter follower, providing a large input resistance for minimizing the loading effects on the gain stage. Bias current for Q_{11} is provided by the current mirror formed by $Q_7$and Q_{12}, through Q_{13} and Q_{14} for minimizing the cross over distortion. Transistors can also be used in place of the two diodes.

The overall voltage gain AV of the op-amp is the product of voltage gain of each stage as given by $A_V=|A_d|$ $|A_2||A_3|$

Where A_d is the gain of the differential amplifier stage, A_2 is the gain of the second gain stage and A_3 is the gain of the output stage.