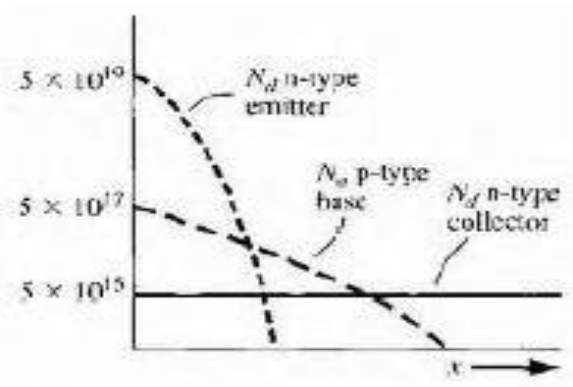
Gummel-Poon Model

The Gummel-Poon model of the BIT considers more physics of the transistor that the Ebers-Moll model. This model can he used if, for example, there is a non-uniform doping concentration in the base.

The electron current density in the base of m npn transistor can be written as

$$J_n = e\mu_n n(x)\mathrm{E} + eD_n \frac{dn(x)}{dx}$$



Impurity concentration profiles of a double-diffused npn bipolar transistor.

An electric field will occur in the base if non uniform doping exists in the base. Electric field can be written as

$$\mathrm{E} = \frac{kT}{e} \cdot \frac{1}{p(x)} \cdot \frac{dp(x)}{dx}$$

where p(x) is the majority carrier hole concentration in the base.
Under low injection, the hole concentration is just the acceptor impurity concentration.
With the doping profile shown in Figure.The electric field is negative (from the collector to the emitter). The direction of this electric field aids the flow of electrons across the base.

Substituting previous Equation we get

$$J_n = e\mu_n n(x) \cdot \frac{kT}{e} \cdot \frac{1}{p(x)} \cdot \frac{dp(x)}{dx} + eD_n \frac{dn(x)}{dx}$$

Using Einstein's relation, we can write Equation in the form

$$J_n = \frac{eD_n}{p(x)}\left(n(x)\frac{dp(x)}{dx} + p(x)\frac{dn(x)}{dx}\right) - \frac{eD_n}{p(x)}\cdot\frac{d(pn)}{dx}$$

It is written in the form of

$$\frac{J_n p(x)}{eD_n} = \frac{d(pn)}{dx}$$

Integrating this eqn through the base

$$\frac{J_n}{eD_n}\int_0^{x_B} p(x)\,dx = \int_0^{x_B}\frac{dp(x)}{dx}\,dx = p(x_B)n(x_B) - p(0)n(0)$$

The integral in the denominator is the total majority carrier charge in the base and is known as the base Gummel number; defined as Q_B.

The hole current density in the emitter of an npn transistor can be expressed as,

$$J_p = \frac{-eD_p n_i^2 \exp(V_{BE}/V_t)}{\int_0^{x_E} n(x')\,dx'}$$

With the doping profile shown in Figure. The electric field is negative (from the collector to the emitter). The direction of this electric field aids the flow of electrons across the base.

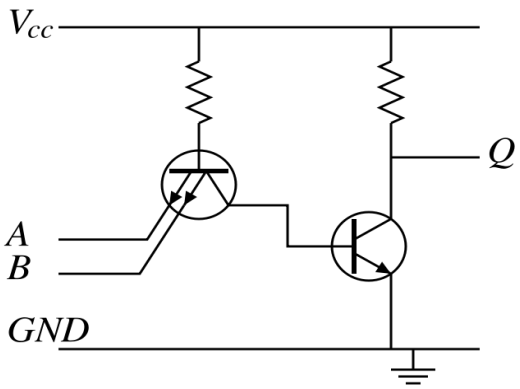
The integral in the denominator is the total majority carrier charge in the emitter and is known as the emitter Gummel number, defined as Q_E.

The Gummel-Poon model can also take into account non ideal effects, such as the Early effect and high-level injection.

If the B-E voltage becomes too large. low injection no longer applies, which leads to high-level injection. In this case, the total hole concentration in the base increases because of the increased excess hole concentration. This means that the base Gummel number will increase.

The Gummel-Poon model can then he used to describe the basic operation of the transistor as well as to describe non ideal effects.

Multi Emitter Transistor (Transistor Transistor Logic)



TTL inputs are the emitters of a multiple-emitter transistor. This IC structure is functionally equivalent to multiple transistors where the bases and collectors are tied together. The output is buffered by a common emitter amplifier.

Inputs both logical ones. When all the inputs are held at high voltage, the base–emitter junctions of the multiple-emitter transistor are reverse-biased. Unlike DTL, a small ‒collector‖ current (approximately 10μA) is drawn by each of the inputs. This is because the transistor is in reverse-active mode. An approximately constant current flows from the positive rail, through the resistor and into the base of the multiple emitter transistor. This current passes through the base-emitter junction of the output transistor, allowing it to conduct and pulling the output voltage low (logical zero).

An input logical zero. Note that the base-collector junction of the multiple-emitter transistor and the base-emitter junction of the output transistor are in series between the bottom of the resistor and ground. If one input voltage becomes zero, the corresponding base-emitter junction of the multiple-emitter transistor is in parallel with these two junctions. A phenomenon called current steering means that when two voltage-stable elements with different threshold voltages are connected in parallel, the current flows through the path with the smaller threshold voltage. As a result, no current flows through the base of the output transistor, causing it to stop conducting and the output voltage becomes high (logical one). During the transition the input transistor is briefly in its active region; so it draws a large current away from the base of the output transistor and thus quickly discharges its base. This is a critical advantage of TTL over DTL that speeds up the transition over a diode input structure.

The main disadvantage of TTL with a simple output stage is the relatively high output resistance at output logical "1" that is completely determined by the output collector resistor. It limits the number of inputs that can be connected (the fanout). Some advantage of the simple output stage is the high voltage level (up to V_{CC}) of the output logical "1" when the output is not loaded.