EC 3352 – DIGITAL SYSTEM DESIGN

UNIT – IV : ASYNCHRONOUS SEQUENTIAL CIRCUITS

4.4 HAZARDS

Hazards are unwanted switching transients that may appear at the output of a circuit because different paths exhibit different propagation delays.

HAZARDS IN COMBINATIONAL CIRCUIT

A hazard is a condition where a single variable change produces a momentary output change when no output change should occur.

- Static-0 hazard – The output may go to 1 when it should remains at 0
- Static-1 hazard – The output may go to 0 when it should remains at 1
- Dynamic hazard – It causes the output to change three or more times when itshould change from 1 to 0 or 0 to 1.

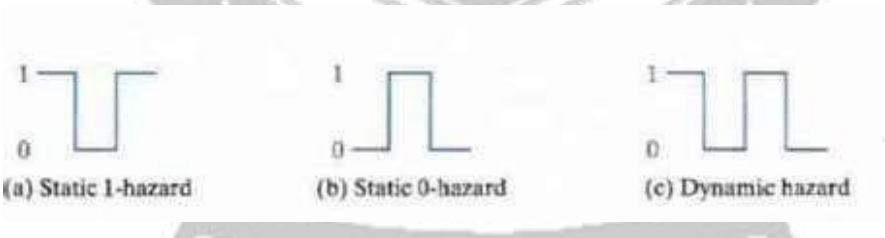

Fig 4.29 – Static and Dynamic Hazard

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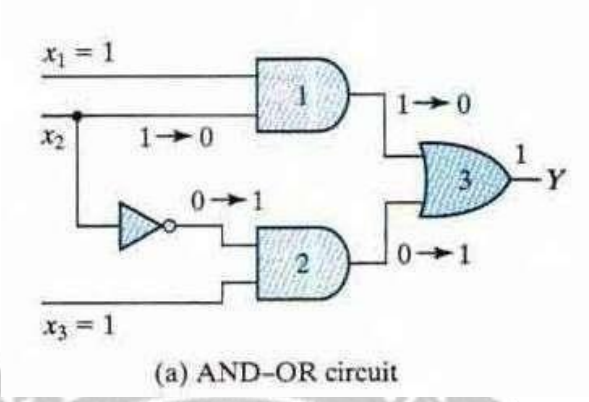

Fig 4.29 – AND –OR Circuit

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The occurrence of the hazard can be detected by inspecting the map of a particularcircuit. The two minterms that cause the hazard are combined into one product term.

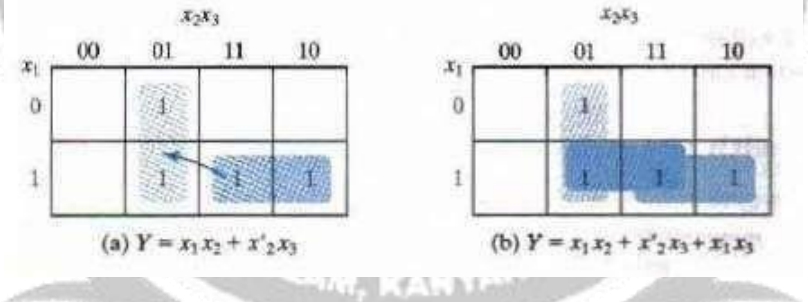

Fig 4.30 – a).With Hazard, b). Without Hazard

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In general, hazard s in combinational circuits can be removed by covering any two minterms that may produce a hazard with a product term common to both. The removal of hazards requires the addition of redundant gates to the circuit.

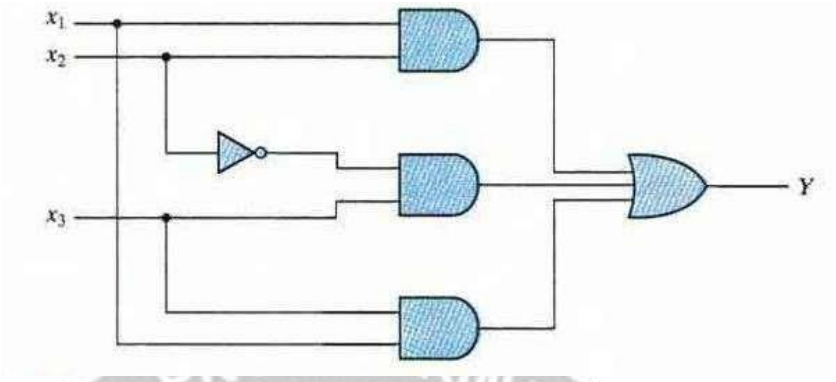

Fig 4.31 – Combinational Circuit without Hazard

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HAZARDS IN SEQUENTIAL CIRCUIT

The hazard can avoid by implementing the circuit with SR latches. A momentary 0 signal applied to the S or R inputs of a NOR latch will have no effect on the state of thecircuit. Similarly, a momentary 1 signal applied to the S and R inputs of a NAND latch will have no effect on the state of the latch.

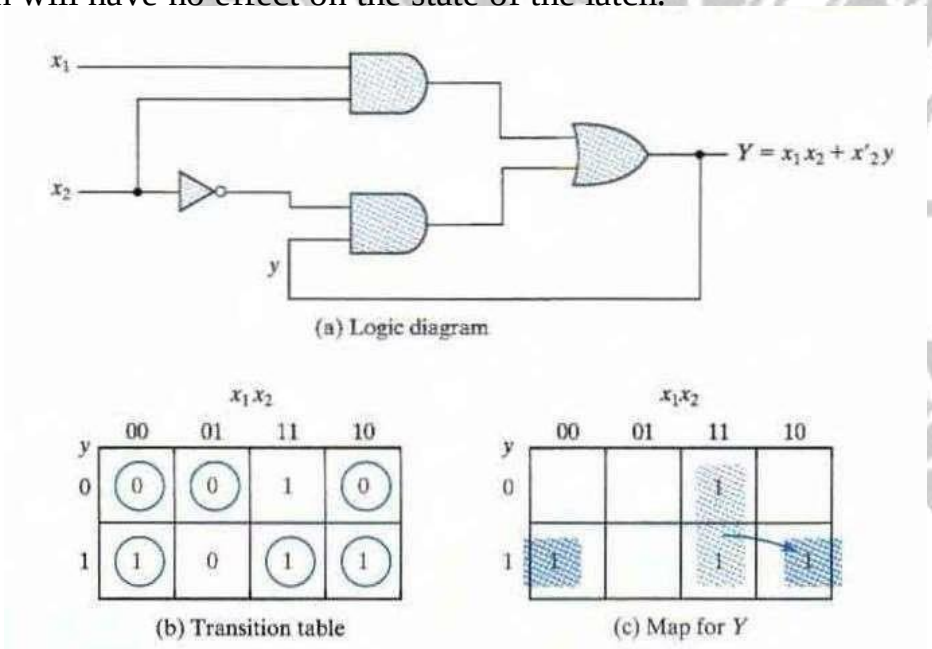

Fig 4.32 – a)logic diagram, b).Transition Table, c). Map for Y Image source from Digital Design by Moris Mano (Page No. 455)

Consider a NAND SR latch with the following Boolean function s for S and R:

$$S = AB + CD$$

$$R = A'C$$

Since this is a NAND latch, we must apply the complemented values to the inputs:

$$S = (AB + CD)' = (AB)' . (CD)'$$

$$R = (AC)'$$

S is generated with two NAND gates and one AND gate. The Boolean functionfor output Q is, $Q= (Q'S)' = [Q'(AB)'(CD)']'$. If output Q is equal to 1, then Q' is equal to
0. If two of the three inputs go momentarily to 1, the NAND gate associated with output Q will remain at 1 because Q' is maintained at 0.

The two NAND gates forming the latch normally have two inputs. However, if the S or R functions contain two or more product terms when expressed as a sum of products, then the corresponding NAND gate of the SR latch will have three or more inputs. Thus, the two terms in the original sum-of-products expression for S are AD and CD, and each is implemented with a NAND gate whose output is applied to the input of the NAND latch. In this way, each state variable requires a two- level circuit of NAND gates. The first level consists of NAND gales that implement each product term in the original Boolean expression of S and R. The second level forms the cross - coupled connection of the SR latch with inputs that come from the outputs of each NAND gatein the first level.

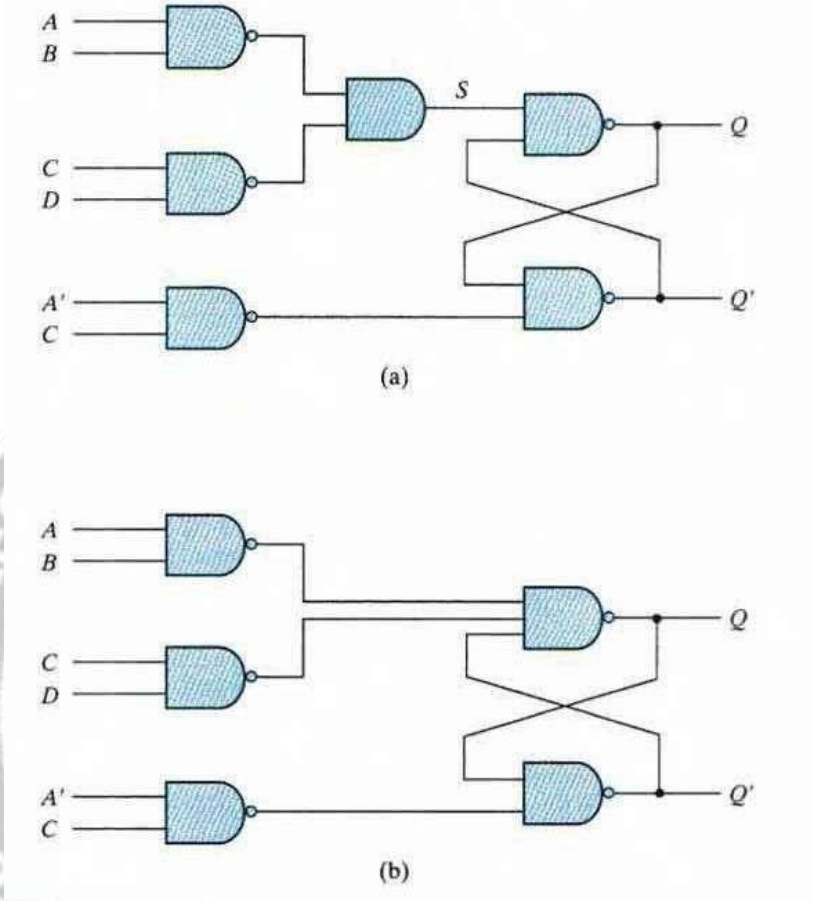

Fig 4.33 – a).Sequential Circuit with Hazard, b). Sequential Circuit without Hazard

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Essentail Hazard

Another type of hazard that may occur in asynchronous sequential circuits is called an essential hazard. This type of hazard is caused by unequal delays along two or more paths that originate from the same input. An excessive delay through an inverter circuit in comparison to the delay associated with the feedback path may cause such a hazard. Essential hazards cannot be corrected by adding redundant gates as in static hazards. The problem that they impose can be corrected by adjusting the amount of delay in the

affected path. To avoid essential hazards, each feedback loop must be handled with individual care to ensure that the delay in the feedback path is long enough compare d with delays of other signals that originate from the input terminals. This problem tends to be specialized, as it depends on the particular circuit used and the size of the delays that are encountered in its various paths.