PROPAGATION DELAY

It is an attempt to reduce the number of transistors required to implement a given logic function, at the cost of reduced robustness and extra power dissipation. The purpose of the PUN in complementary CMOS is to provide a conditional path between VDD and the output when the PDN is turned off. In ratioed logic, the entire PUN is replaced with a single unconditional load device that pulls up the output for a high output (Figure 5.a). Instead of a combination of active pull-down and pull-up networks, such a gate consists of an NMOS pull- down network that realizes the logic function, and a simple load device. Figure 5.b shows an example of ratioed logic, which uses a grounded PMOS load and is referred to as a pseudo- NMOS gate.

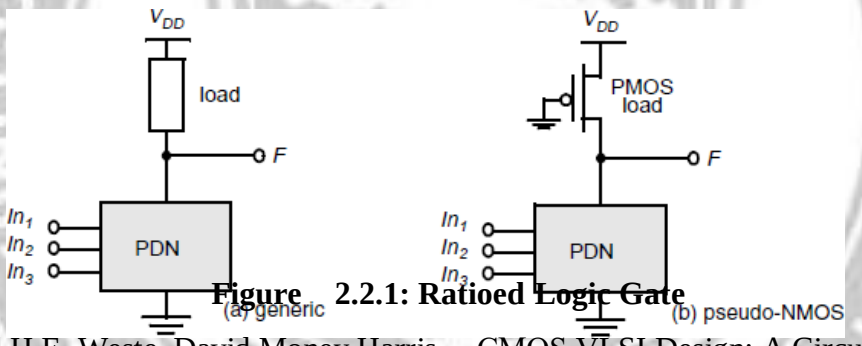

Figure 2.2.1: Ratioed Logic Gate

[Source :Neil H.E. Weste, David Money Harris —CMOS VLSI Design: A Circuits and Systems Perspective…]

The clear advantage of pseudo-NMOS is the reduced number of transistors (N+1versus 2N for complementary CMOS). The nominal high output voltage (VOH) for this gate is VDD since the pull-down devices are turned off when the output is pulled high(assuming that VOL is below VTn). On the other hand, the **nominal low output voltage is not 0 V** since there is a fight between the devices in the PDN and the grounded PMOS load device. This results in reduced noise margins and more importantly static power dissipation.

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The sizing of the load device relative to the pull-down devices can be used to trade-off parameters such a noise margin, propagation delay and power dissipation. Since the voltage swing on the output and the overall functionality of the gate depends upon the ratio between the NMOS and PMOS sizes, the circuit is called ratioed. This is in contrast to the ratioless logic styles, such as complementary CMOS, where the low and high levels do not depend upon transistor sizes.

Computing the dc-transfer characteristic of the pseudo-NMOS proceeds along paths similar to those used for its complementary CMOS counterpart. The value of VOL is obtained by equating the currents through the driver and load devices for Vin = VDD. At this operation point, it is reasonable to assume that the NMOS device resides in linear mode (since the output should ideally be close to 0V), while the PMOS load is saturated.

$$k_n\left((V_{DD}-V_{Tn})V_{OL}-\frac{V_{OL}^2}{2}\right) = k_p\left((-V_{DD}-V_{Tp})\cdot V_{DSAT}-\frac{V_{DSAT}^2}{2}\right)$$

Assuming that VOL is small relative to the gate drive (VDD-VT) and that VTn is equal to VTp in magnitude, VOL can be approximated as:

$$V_{OL} \approx \frac{k_p(-V_{DD}-V_{Tp})\cdot V_{DSAT}}{k_n(V_{DD}-V_{Tn})} \approx \frac{\mu_p \cdot W_p}{\mu_n \cdot W_n}\cdot |V_{DSAT}|$$

In order to make VOL as small as possible, the PMOS device should be sized much smaller than the NMOS pull-down devices. Unfortunately, this has a negative impact on the propagation delay for charging up the output

node since the current provided by the PMOS device is limited.

A major disadvantage of the pseudo-NMOS gate is the static power that is dissipated when the output is low through the direct current path that exists between VDD and GND. The static power consumption in the low-output mode is easily derived.

$$P_{low} = V_{DD} I_{low} \approx V_{DD} \cdot k_p \left((-V_{DD} - V_{Tp}) \cdot V_{DSATp} - \frac{V_{DSATp}^2}{2} \right)$$

Dynamic CMOS design

Dynamic circuits overcome these drawbacks by using a clocked pull-up transistor rather than a pMOS that is always ON. Dynamic circuit operation is divided into two modes, as shown in Figure 9.22. During Precharge, the clock K is 0, so the clocked pMOS is ON and initializes the output Y high. During evaluation, the clock is 1 and the clocked pMOS turns OFF. The output may remain high or may be discharged low through the pull down network. Dynamic circuits require careful clocking, consume significant dynamic power, and are sensitive to noise during evaluation.

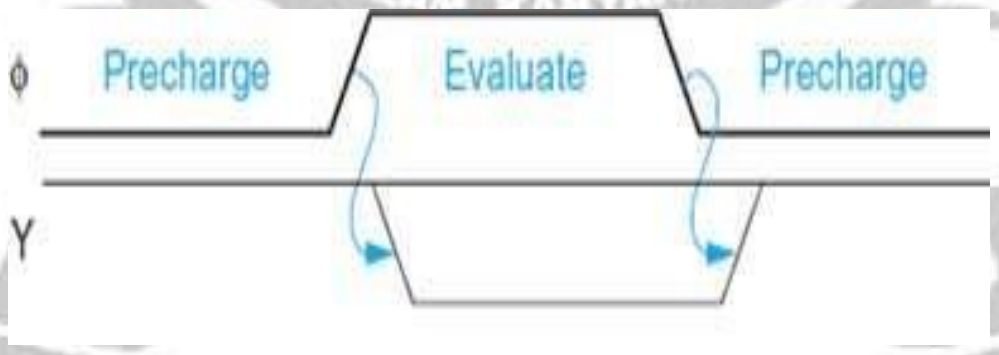

Figure 2.2.2: Precharge and Evaluation of Dynamic gates

[Source :Neil H.E. Weste, David Money Harris —CMOS VLSI Design: A Circuits and Systems Perspective…]

If the input A is 1 during Precharge, contention will take place because both the pMOS and nMOS transistors will be ON. When the input cannot be guaranteed to be 0 during Precharge, an extra clocked evaluation transistor can be added to the bottom of the nMOS stack to avoid contention as shown in Figure 9.23. The extra transistor is sometimes called a foot. Figure 9.2 shows generic footed and unfooted gates.

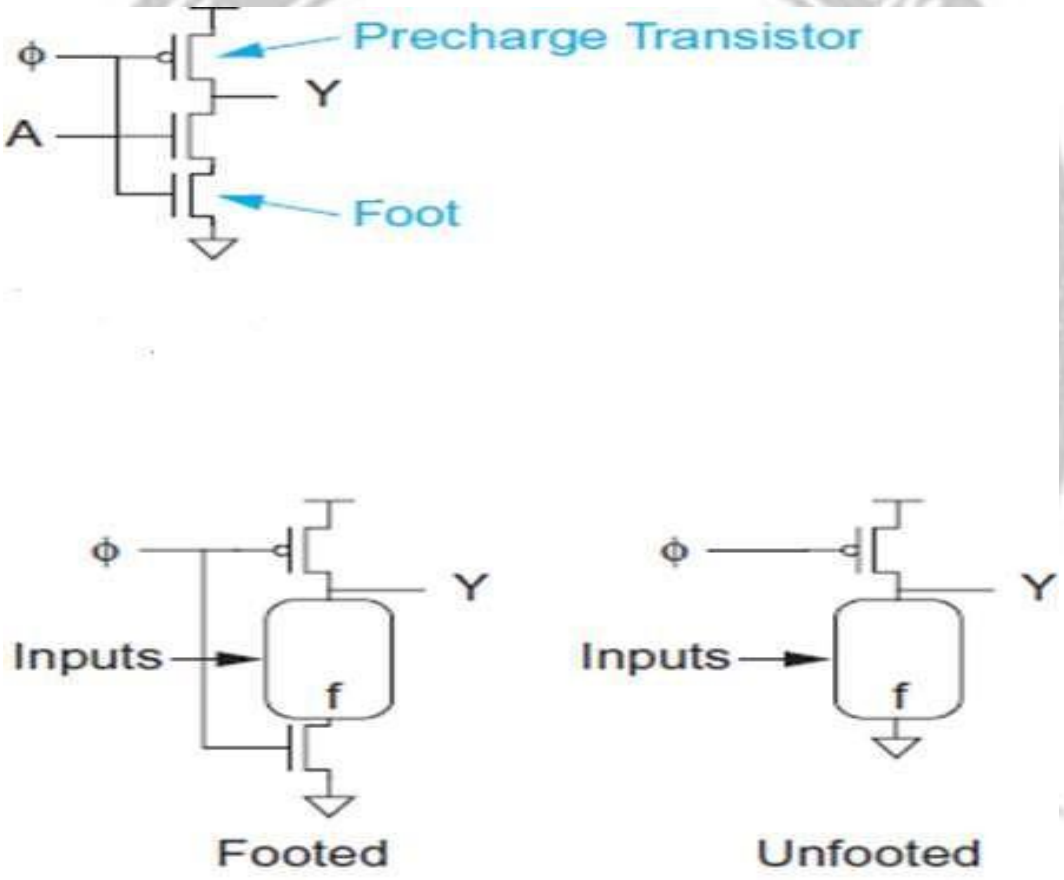

Figure 2.2.3: Footed and Unfooted Dynamic gates

[Source :Neil H.E. Weste, David Money Harris —CMOS VLSI Design: A Circuits and Systems Perspective…]

Figure 2.2.3 estimates the falling logical effort of both footed and unfooted dynamic gates. Footed gates have higher logical effort than their unfooted counterparts but are still an improvement over static logic.

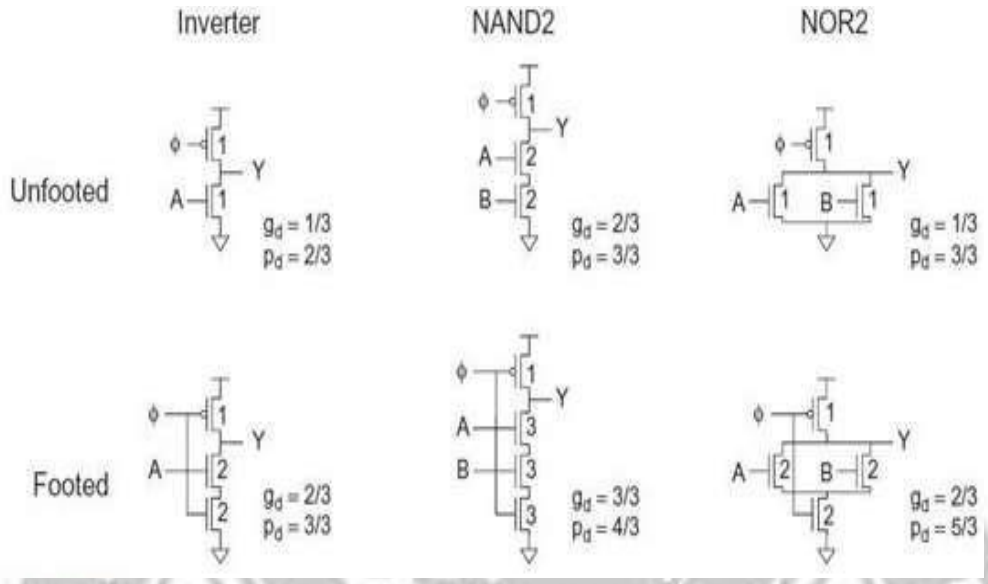

Figure 2.2.4: Catalog of Dynamic gates

[Source :Neil H.E. Weste, David Money Harris ―CMOS VLSI Design: A Circuits and Systems Perspective…]

A fundamental difficulty with dynamic circuits is the monotonicity requirement. While a dynamic gate is in evaluation, the inputs must be monotonically rising. That is, the input can start LOW and remain LOW, start LOW and rise HIGH, start HIGH and remain HIGH, but not start HIGH and fall LOW. Figure

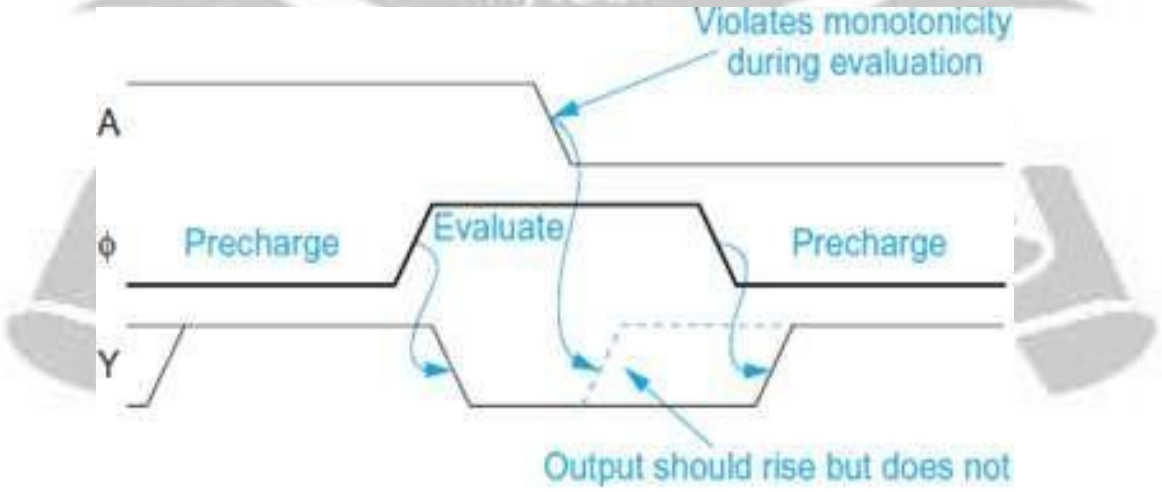

Figure 2.2.5: Monotonicity Problem

[Source :Neil H.E. Weste, David Money Harris ―CMOS VLSI Design: A Circuits and

Systems Perspective…]

shows waveforms for a footed dynamic inverter in which the input violates monotonicity.

The output of a dynamic gate begins HIGH and monotonically falls LOW during evaluation. This monotonically falling output X is not a suitable input to a second dynamic gate expecting monotonically rising signals, as shown in Figure 9.27. Dynamic gates sharing the same clock cannot be directly connected.

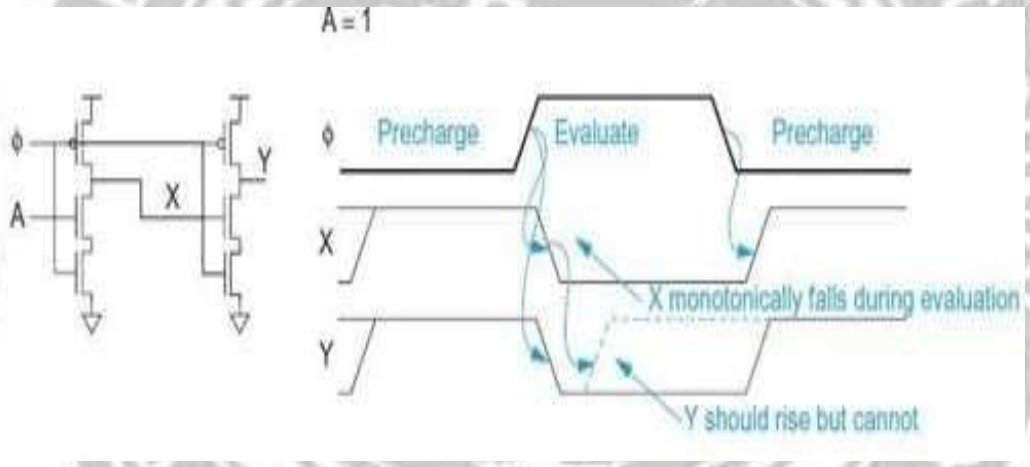

Figure 2.2.6: Incorrect Connection of Dynamic Gates

[Source :Neil H.E. Weste, David Money Harris ―CMOS VLSI Design: A Circuits and Systems Perspective…]

Advantages

- Lower input capacitance
- No contention during switching
- Zero static power dissipation

Disadvantages

- Require careful clocking

- Consume significant dynamic power
- Sensitive to noise

Applications

- Used in wide NOR functions
- Used in multiplexers