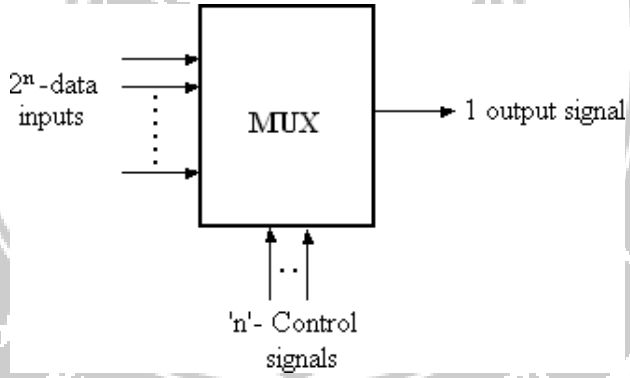
MULTIPLEXER: (Data Selector)

A ***Multiplexer*** or *MUX*, is a combinational circuit with more than one input line, one output line and more than one selection line. A multiplexer selects binary information present from one of many input lines, depending upon the logic status of the selection inputs, and routes it to the output line. Normally, there are 2^n input lines and n selection lines whose bit combinations determine which input is selected. The multiplexer is often labeled as MUX in block diagrams.

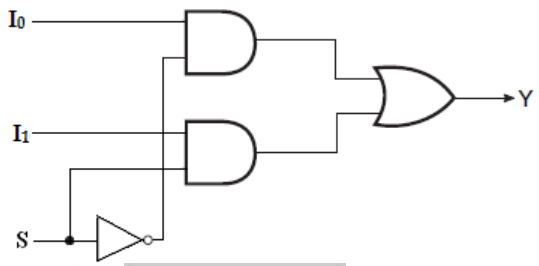
A multiplexer is also called a **data selector**, since it selects one of many inputs and steers the binary information to the output line.



Block diagram of Multiplexer

2-to-1- line Multiplexer:

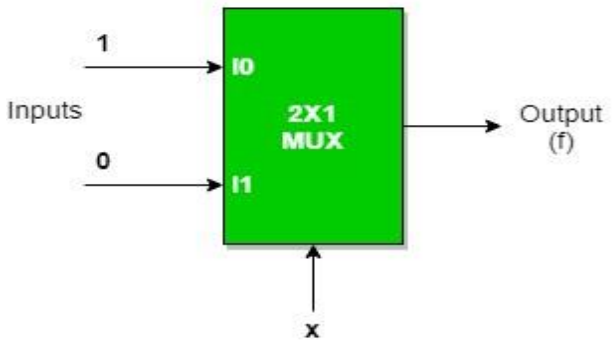
The circuit has two data input lines, one output line and one selection line, S. When S= 0, the upper AND gate is enabled and I_0 has a path to the output. When S=1, the lower AND gate is enabled and I_1 has a path to the output



Logic diagram

The multiplexer acts like an electronic switch that selects one of the two sources.

Truth Table



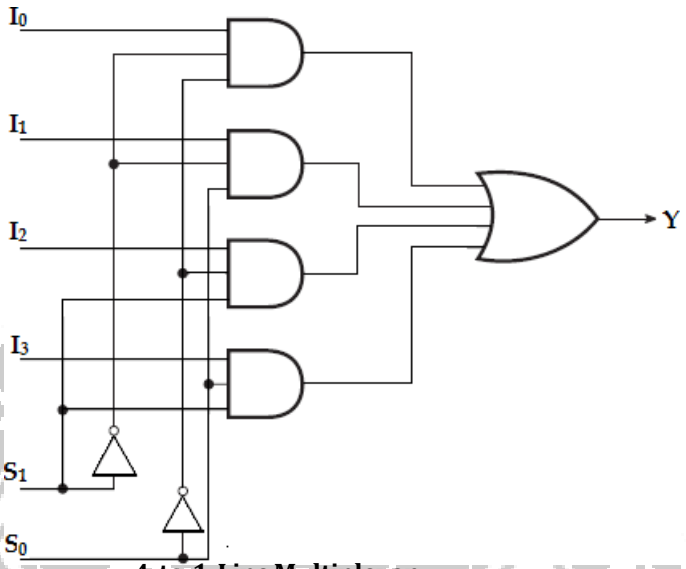
Truth Table

x	f
0	1
1	0

4-to-1-line Multiplexer

A 4-to-1-line multiplexer has four (2^n) input lines, two (n) select lines and one output line. It is the multiplexer consisting of four input channels and information of one of the channels can be selected and transmitted to an output line according to the select inputs combinations. Selection of one of the four input channel is possible by two selection inputs.

Each of the four inputs I_0 through I_3, is applied to one input of AND gate. Selection lines S_1 and S_0 are decoded to select a particular AND gate. The outputs of the AND gate are applied to a single OR gate that provides the 1-line output.



4-to-1-Line Multiplexer

Function table:

S_1	S_0	Y
0	0	I_0
0	1	I_1
1	0	I_2
1	1	I_3

To demonstrate the circuit operation, consider the case when S_1S_0= 10. The AND gate associated with input I_2 has two of its inputs equal to 1 and the third input connected to I_2. The other three AND gates have at least one input equal to 0, which makes their outputs equal to 0. The OR output is now equal to the value of I_2, providing a path from the selected input to the output.

The data output is equal to I_0 only if S_1= 0 and S_0= 0; Y= $I_0S_1'S_0'$.

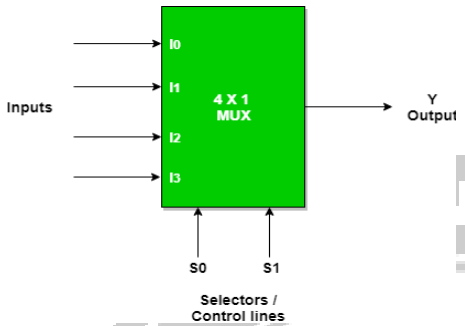
The data output is equal to I_1 only if S_1= 0 and S_0= 1; Y= $I_1S_1'S_0$. The data output is equal to I_2 only if S_1= 1 and S_0= 0; Y= $I_2S_1S_0'$. The data output is equal to I_3 only if S_1= 1 and S_0= 1; Y= $I_3S_1S_0$.

When these terms are ORed, the total expression for the data output is,

$$\mathbf{Y= I_0S_1'S_0'+ I_1S_1'S_0 +I_2S_1S_0'+ I_3S_1S_0}.$$

As in decoder, multiplexers may have an enable input to control the operation of the unit. When the enable input is in the inactive state, the outputs

are disabled, and when it is in the active state, the circuit functions as a normal multiplexer.



Truth Table

S0	S1	Y
0	0	I0
0	1	I1
1	0	I2
1	1	I3

So, final equation,

$Y = S0'.S1'.I0 + S0'.S1.I1 + S0.S1'.I2 + S0.S1.I3$