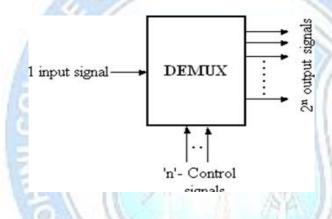
## **DEMULTIPLEXER**

Demultiplexer means one into many. Demultiplexing is the process of taking information from one input and transmitting the same over one of several outputs.

A demultiplexer is a combinational logic circuit that receives information on a single input and transmits the same information over one of several (2<sup>n</sup>) output lines.

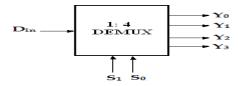


Block diagram of demultiplexer

The block diagram of a demultiplexer which is opposite to a multiplexer in its operation is shown above. The circuit has one input signal, 'n' select signals and 2<sup>n</sup> output signals. The select inputs determine to which output the data input will be connected. As the serial data is changed to parallel data, i.e., the input caused to appear on one of the n output lines, the demultiplexer is also called a "data distributer" or a "serial-to-parallel converter".

## 1-to-4 line Demultiplexer

A 1-to-4 demultiplexer has a single input, Din, four outputs (Y0 to Y3) and twoselect inputs (S1 and S0)



The input variable  $D_{in}\, has \, a$  path to all four outputs, but the input information is DEVIVISALAKSHI.G-AP/CSE/RCET

CS3351-DIGITAL PRINCIPLES AND COMPUTER ORGANIZATION

### ROHINI COLLEGE OF ENGINEERING AND TECHNOLOGY

directed to only one of the output lines. The truth table of the 1-to-4 demultiplexer is shown below

Enable	$S_1$	$S_0$	Din	Y <sub>0</sub>	<b>Y</b> <sub>1</sub>	$\mathbf{Y}_2$	<b>Y</b> <sub>3</sub>
0	X	X	X	0	0	0	0
1	0	0	0	0	0	0	0
1	0	0	1	1	0	0	0
1	0	1	0	0	0	0	0
1	0	1	1	0	1	0	0
1	1	0	0	0	0	0	0
1	1	0	1	0	0	1	0
1	1	1	0	0	0	0	0
/51//	1	1	1	0	0	0	1

Truth table of 1-to-4 demultiplexer

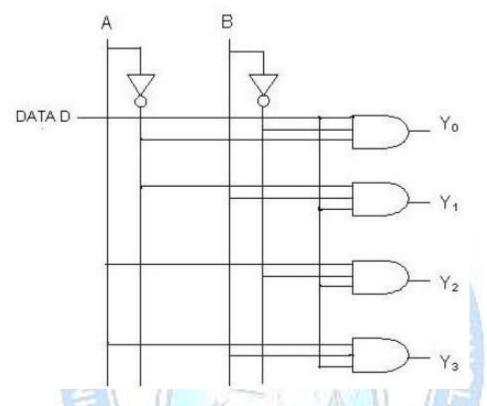
From the truth table, it is clear that the data input,  $D_{in}$  is connected to the output  $Y_0$ , when  $S_1$ = 0 and  $S_0$ = 0 and the data input is connected to output  $Y_1$  when  $S_1$ = 0 and  $S_0$ = 1. Similarly, the data input is connected to output  $Y_2$  and  $Y_3$  when  $S_1$ = 1 and  $S_0$ = 0 and when  $S_1$ = 1 and  $S_0$ = 1, respectively. Also, from the truth table, the expression for outputs can be written as follows,

$$Y_0 = S_1'S_0'D_{in}$$

$$Y_1 = S_1'S_0D_{in}$$

$$Y_2 = S_1 S_0' D_{in}$$

$$Y_3 = S_1 S_0 D_{in}$$



Logic diagram of 1-to-4 demultiplexer

Now, using the above expressions, a 1-to-4 demultiplexer can be implemented using four 3-input AND gates and two NOT gates. Here, the input data line  $D_{\rm in}$ , is connected to all the AND gates. The two select lines  $S_1$ ,  $S_0$  enable only one gate at atime and the data that appears on the input line passes through the selected gate to the associated output line.

# 1-to-8 Demultiplexer

A 1-to-8 demultiplexer has a single input,  $D_{in}$ , eight outputs ( $Y_0$  to  $Y_7$ ) and three select inputs ( $S_2$ ,  $S_1$  and  $S_0$ ). It distributes one input line to eight output linesbased on the select inputs. The truth table of 1-to-8 demultiplexer is shown below.

Din	$S_2$	$S_1$	$S_0$	<b>Y</b> <sub>7</sub>	<b>Y</b> <sub>6</sub>	<b>Y</b> <sub>5</sub>	<b>Y</b> <sub>4</sub>	<b>Y</b> <sub>3</sub>	$\mathbf{Y}_2$	<b>Y</b> <sub>1</sub>	Y <sub>0</sub>
0	X	X	X	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0	0	0	0	1
1	0	0	1	0	0	0	0	0	0	1	0

### ROHINI COLLEGE OF ENGINEERING AND TECHNOLOGY

1	0	1	0	0	0	0	0	0	1	0	0
1	0	1	1	0	0	0	0	1	0	0	0
1	1	0	0	0	0	0	1	0	0	0	0
1	1	0	1	0	0	1	0	0	0	0	0
1	1	1	0	0	1	0	0	0	0	0	0
1	1	1	1	1	0	0	0	0	0	0	0

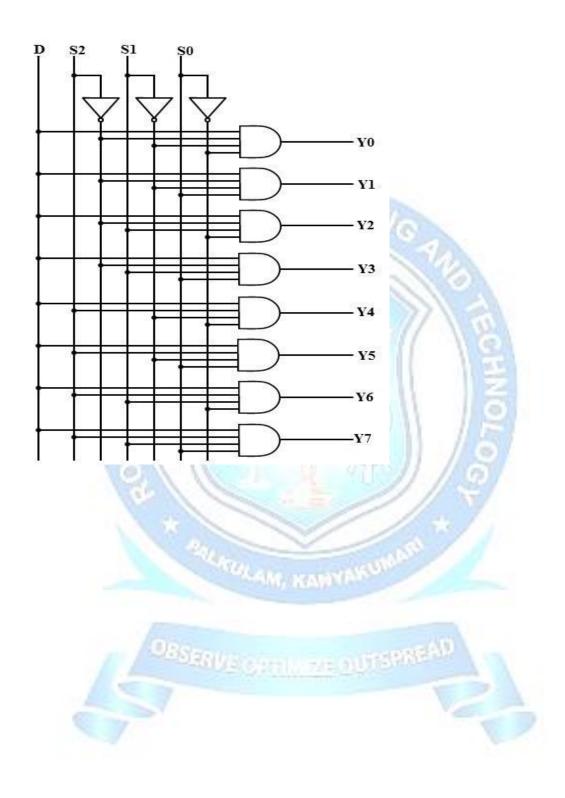
## Truth table of 1-to-8 demultiplexer

From the above truth table, it is clear that the data input is connected with one of the eight outputs based on the select inputs. Now from this truth table, the expression for eight outputs can be written as follows:

$$\begin{array}{lll} Y_0 = & S_2 ' S_1 ' S_0 ' D_{\rm in} & Y_4 = & S_2 \, S_1 ' S_0 ' D_{\rm in} \\ Y_1 = & S_2 ' S_1 ' S_0 D_{\rm in} & Y_5 = & S_2 \, S_1 ' S_0 D_{\rm in} \\ Y_2 = & S_2 ' S_1 S_0 ' D_{\rm in} & Y_6 = & S_2 \, S_1 S_0 ' D_{\rm in} \\ Y_3 = & S_2 ' S_1 S_0 D_{\rm in} & Y_7 = & S_2 S_1 S_0 D_{\rm in} \end{array}$$

Now using the above expressions, the logic diagram of a 1-to-8 de multiplexer can be drawn as shown below. Here, the single data line,  $D_{in}$  is connected to all the eight AND gates, but only one of the eight AND gates will be enabled by the select input lines. For example, if  $S_2S_1S_0$ = 000, then only AND gate-0 will be enabled and thereby the data input,  $D_{in}$  will appear at  $Y_0$ . Similarly, the different combinations of the select inputs, the input  $D_{in}$  will appear at the respective output.

## ROHINI COLLEGE OF ENGINEERING AND TECHNOLOGY



DEVIVISALAKSHI.G-AP/CSE/RCET CS3351-DIGITAL PRINCIPLES AND COMPUTER ORGANIZATION