POWER BJT

Bipolar Junction Transistor (BJT) is a three terminal, three layer, two junction semiconductor device. Emitter(E), Base(B) and Collector(C) are the three terminals of the device.

Symbol: The symbol of the Power BJT is same as signal level transistor.

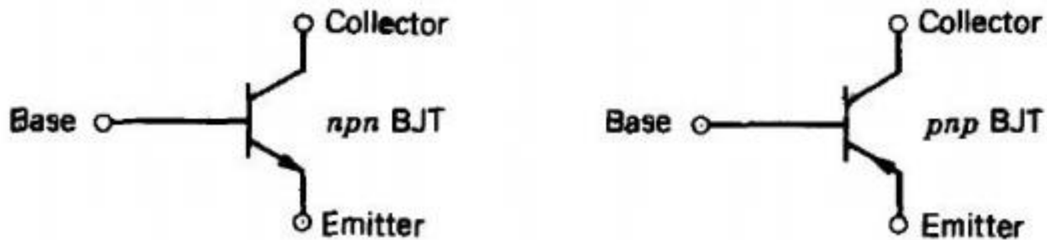

Figure 1 Symbol of power BJT

Structure

The construction of the Power Transistor is different from the signal transistor as shown in the following figure 2.. The n- layer is added in the power BJT which is known as drift region.

- A Power BJT has a four layer structure of alternating P and N type doping as shown in above npn transistor.

It has three terminals labeled as Collector, Base, Emitter.

- In most of Power Electronic applications, the Power Transistor works in Common Emitter configuration.
- ie, Base is the input terminal, the Collector is the output terminal and the Emitter is common between input and output.
- In power switches npn transistors are most widely used than pnp transistors.
- The thickness of the dirft region determines the breakdown voltage of the Power transistor.
- The characteristics of the device is determined by the doping level in each of the layers and the thickness of the layers.

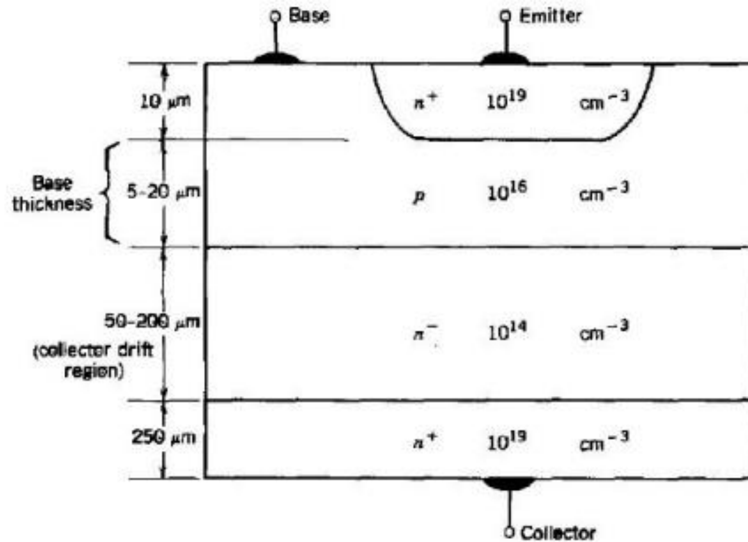

Figure 2. Structure of Power BJT

VI Characteristics

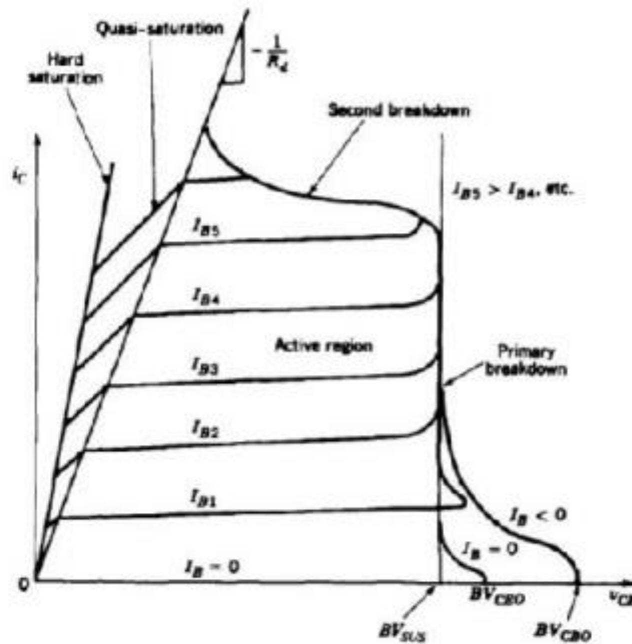

Figure 3. VI Characteristics Power BJT

- The VI characteristics of the Power BJT is different from signal level transistor.
- The major differences are Quasi saturation region & secondary breakdown region.

- The Quasi saturation region is available only in Power transistor characteristic not in signal transistors. It is because of the lightly doped collector drift region present in Power BJT.
- The primary breakdown is similar to the signal transistor's avalanche breakdown
- Operation of device at primary and secondary breakdown regions should be avoided as it will lead to the catastrophic failure of the device.

POWER MOSFET

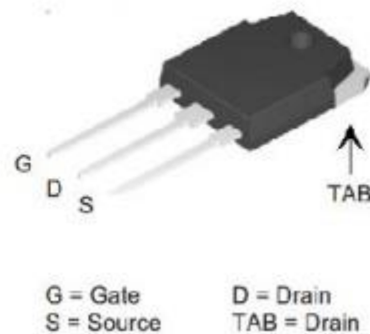

Figure 1. IC model for Power MOSFET

A metal-oxide-semiconductor field-effect transistor (MOSFET) is developed by combining the areas of field-effect concept and MOS technology. The Conventional planar MOSFET has the restriction of handling the high power. In high power applications, the Double-diffused vertical MOSFET or VMOS is used which is simply known as Power MOSFET.

Power MOSFET

- The Power MOSFET is the three terminal (Gate, Drain and Source), four layer ($n^{+}pnn^{+}$), Unipolar (only majority carriers in conduction) semiconductor device.
- The MOSFET is a majority carrier device, and as the majority carriers have no recombination delays, the MOSFET achieves extremely high bandwidths and switching times.
- The gate is electrically isolated from the source, and while this provides the MOSFET with its high input impedance, it also forms a good capacitor.
- MOSFETs do not have secondary breakdown area, their drain to source resistance has a positive temperature coefficient, so they tend to be self protective.
- It has very low ON resistance and no junction voltage drop when forward biased. These features make MOSFET an extremely attractive power supply switching device.

Symbol

The symbol for n-channel MOSFET is given below. The direction of the arrow on the lead that goes to the body region indicates the direction of current flow. As this is the symbol for n channel MOSFET, the arrow is inwards. For p-channel MOSFET, the arrow will be towards outside.

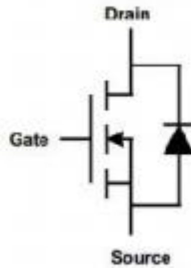

Figure 2. Symbol of Power MOSFET

STRUCTURE

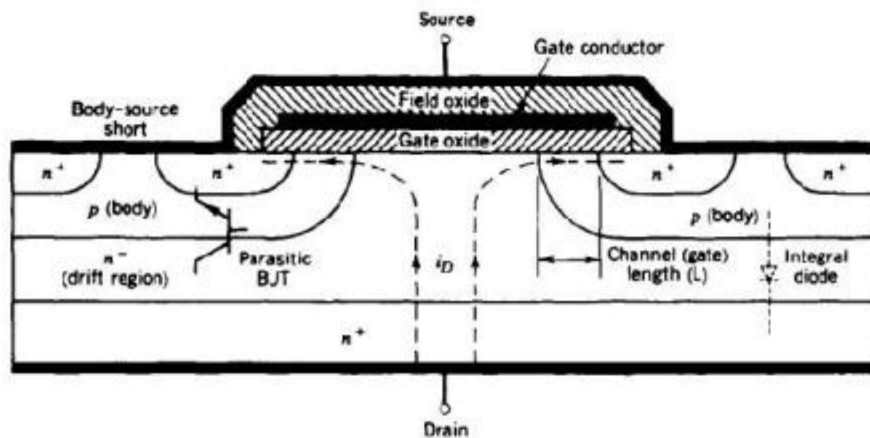

Figure 3. Structure of Power MOSFET

- The Power MOSFET has a vertically oriented four layer structure of alternating P and N type ($n^+pn^-n^+$) layers.
- The P type middle layer is called as body of MOSFET. In this region , the channel is formed between source and drain.
- The n- layer is called as drift region, which determines the breakdown voltage of the device. This n- region is present only in Power MOSFETs not in signal level MOSFET.
- The gate terminal is isolated from body by silicon dioxide layer.
- When the positive gate voltage is applied with respect to source, the n-type channel is formed between source to drain. As shown in the figure 3.there is a parasitic npn BJT between source and drain.
- To avoid this BJT turns on, the p-type body region is shorted to source region by overlapping the source metallization on to the p type body. The result is a parasitic diode which is formed between drain to source terminals. This integral diode plays an important role in half and full bridge converter circuits.

Characteristics

`The VI characteristics of n-channel enhancement mode MOSFET.

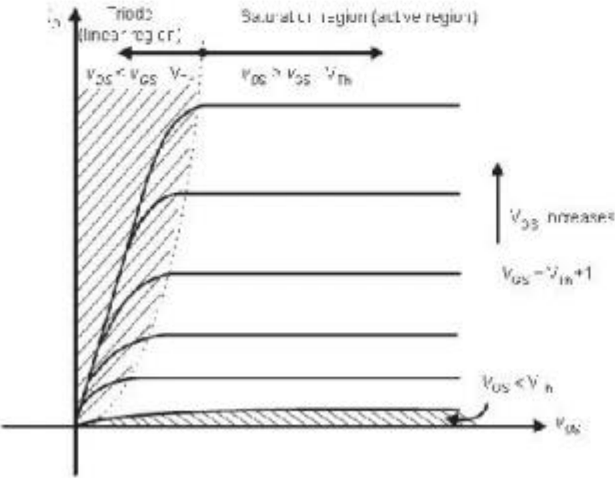

Figure 4. V-I characteristics of n-channel enhancement mode MOSFET

DOUBLE-DIFFUSED MOS (DMOS)

The figure 1. shows a double-diffused MOS (DMOS) structure. T he channel length, L, is controlled by the junction de pth produced by the n^+ and p-type diffusions underneath the gate oxide. L is also the lateral distance between the n^+ p junction and the p-n substrate junction. The channel length can be made to a smaller distance of about 0.5 micro meters. Thus, this process is similar to the situation with resspect to the base width of a double-diffused bipolar transistor. When a fairly large positive voltage is applied to the gate [$>V_{TH}$], it will cause the inversion of the p-substrate region underneath thhe gate to n- type , and the n-type surface inversion layer that is produced will act as a conducting channel for the flow of electrons from sou rce to drain.

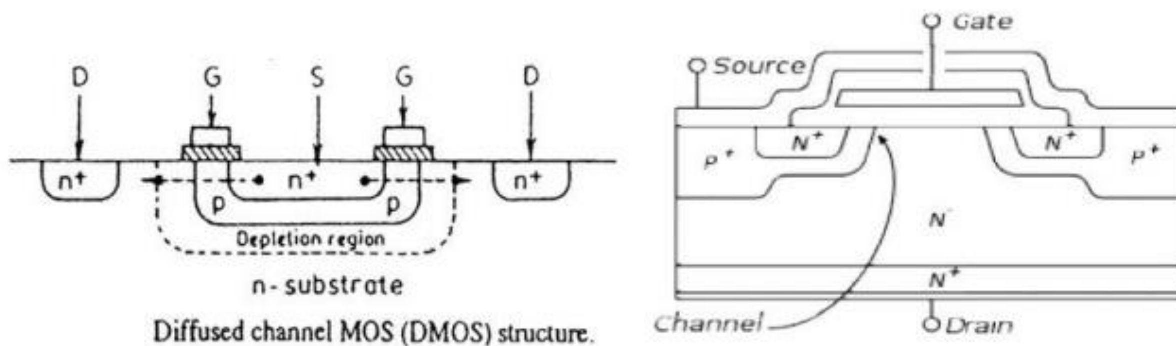

Figure 1. Double-Diffused MOS (DMOS) Structure

From the structure it is known that the n-type substrate is very lightly doped. This will help in making enough space for thee expansion of the depletion region between the p-type diffusion region and the n^+ drain contact region. Due to this, the breakdown voltage w ill become higher between the drain and source.