3.4 MOS

Mos transistors are built on a p-type substrate of moderate doping. Source and drain are formed by diffusing heavily doped n-type impurities (n+)adjacent to the gate. A layer of silicon dioxide (SiO_2) or glass is place over the substrate in between the source and drain. Over SiO_2, a layer of polycrystalline silicon or polysilicon is formed, from which the gate terminal is taken.

The following figure shows the structure and symbol of nMOS transistor.R

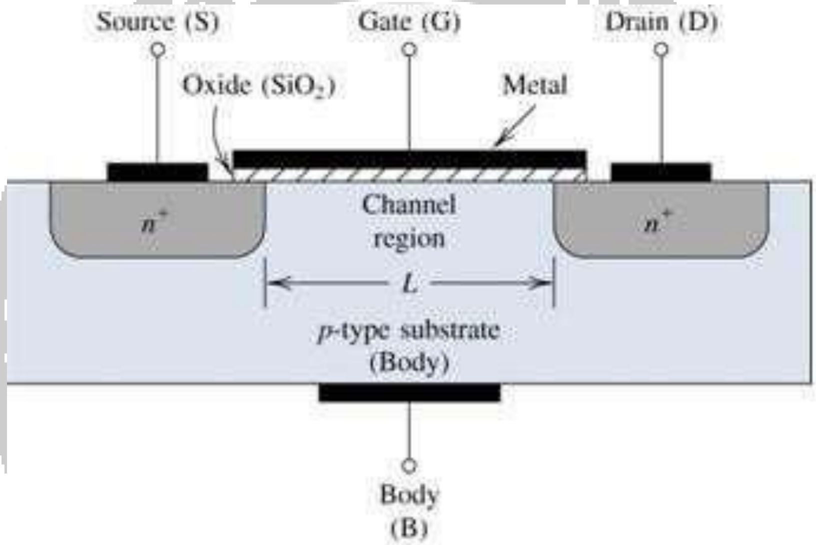

Fig: 3.1 MOS transistor.

[Source: R.Jacob Baker, CMOS Circuit Design, Layout and Simulation...]

Threshold Voltage (V_t)

It can be defined as the voltage applied between the gate and the source of a MOS device (V_{gs}) below which the drain-to-source current (I_{ds}) "effectively" drops to zero. V_t depends on thefollowing:

- Gate conduction material
- Gate insulation material
- Gate insulator thickness
- Channel doping
- Impurities at the silicon-insulator interface
- Voltage between the source and the substrate, V_{sb}.

Modes of operation of MOS Transistor:

The following are the three modes of operation of nMOS transistor:

1. Accumulation mode
2. Depletion mode
3. Inversion mode

a. Accumulation Mode

In this mode a negative voltage is applied to the gate. So there is negative charge on the gate. The mobile positively charged holes are attracted to the region beneath the gate.

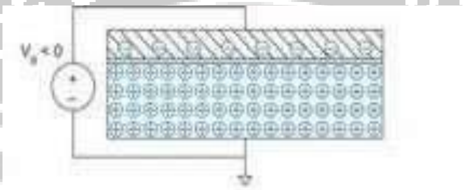

Fig: 3.2 Accumulation Mode.

[Source: R.Jacob Baker, CMOS Circuit Design, Layout and Simulation...]

b. Depletion Mode:

In this mode a low positive voltage is applied to the gate. This results in some positive charge on the gate. The holes in the body are repelled from the region directly beneath the gate.

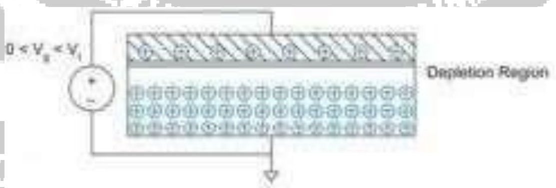

Fig: 3.3 Depletion Mode.

[Source: R.Jacob Baker, CMOS Circuit Design, Layout and Simulation...]

c. Inversion Mode:

In this mode, a higher positive potential exceeding a critical threshold voltage is applied. This attracts more positive charge to the gate. The holes are repelled further and a small number of free electrons in the body are attracted to the region beneath the gate. This conductive layer of electrons in the p-type body is called the inversion layer.

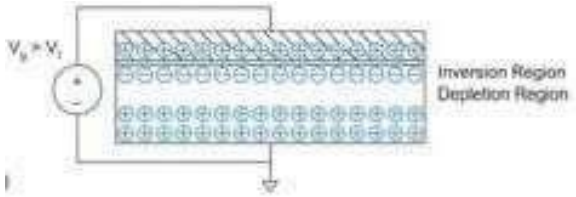

Fig: 3.4 Inversion Mode.

[Source: R.Jacob Baker, CMOS Circuit Design, Layout and Simulation...]

Behavior of nMOS with different voltages:

The Behavior of nMOS with different voltages can be classified into the following three cases and is illustrated in below figure.

i. Cut-off region

ii. Linear region

iii. Saturation region

a. Cut-off region:-

In this region $V_{gs} < V_t$ .The source and drain have free electrons. The body has free holes but no free electrons. The junction between the body and the source or drain is reverse biased. So no current will flow. This mode of operation is called cut-off.

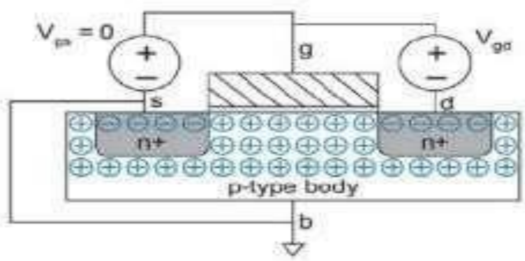

Fig: 3.5 Cut off region.

[Source: R.Jacob Baker, CMOS Circuit Design, Layout and Simulation...]

Linear region:-

In this region $V_{gs} > V_t$ .Now an inversion region of electrons called the channel connects the source and drain. This creates a conductive path between source and drain. The number of carriers and the conductivity increases with the gate voltage. The potential difference between drain and source is $V_{ds} = V_{gs} - V_{gd}$. If $V_{ds}=0$,there is no electric field tending to push current from drain to source.

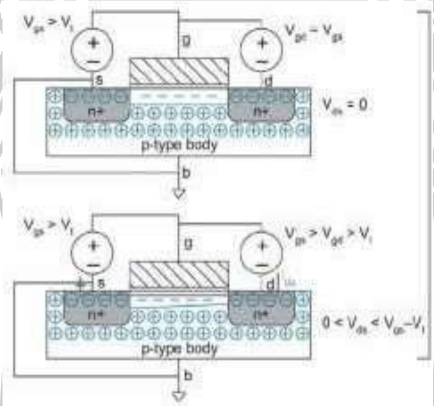

Fig: 3.6 Linear region.

[Source: R.Jacob Baker, CMOS Circuit Design, Layout and Simulation...]

b. Saturation region:-

In this region V_{ds} becomes sufficiently larger than $V_{gd} < V_t$, the channel is no longer inverted near the drain and becomes pinched off .Above this drain voltage, the I_{ds} is controlled only by the gate voltage. This mode is called saturation mode.

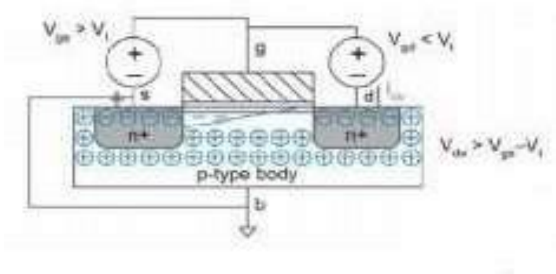

Fig:3.7 Saturation region.

[Source: R.Jacob Baker, CMOS Circuit Design, Layout and Simulation...]