MOS LOGIC FAMILIES

In most designs, there exist many logic paths called critical paths. These paths are recognized by a timing analyzer or circuit simulator. Critical paths are affected by the following four levels.

i. Architectural level
ii. Logic level
iii. Circuit level
iv. Layout level

Propagation delay time (tpd) or max time is the maximum time from the input crossing 50%to the output crossing 50%.The delay can be estimated by the following ways,

i. RC delay models
ii. Linear delay models
iii. Logic efforts
iv. Parasitic delay

1. RC delay models:

The delay of logic gate is computed as the product of RC,where R is the effective driver resistance and C the load capacitance. Logic gates use minimum –length devices for least delay, area and power consumption. The delay of a logic gate depends on the transistor width in the gate and the capacitance of the load.

Effective Resistance and Capacitance:

An NMOS transistor with width of one unit has effective esistance R An PMOS transistor with width of one unit has effective resistance 2R Capacitance consists of gate capacitance cg and source/diffusion capacitance c diff .in most processes cg is equal to c diff , c g and cdiff are proportional to transistor width.

Diffusion capacitance layout effects:

To reduce the diffusion capacitance in the layout, diffusion nodes are shared. Uncontacted nodes have less capacitance. Diffusion capacitance depends on the layout.

2. Elmore delay model:

Elmore delay model estimates the delay of an RC ladder .this is equal to the sum over each node in the ladder of the resistance between the node and supply multiplied by capacitance on the node.

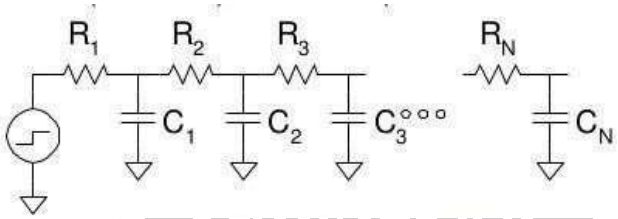

Fig 1.5.1: RC ladder for Elmore Delay Model

[Source: Neil H.E. Weste, David Money Harris —CMOS VLSI Design..]

3. Linear delay model:

The propagation delay of a gate is d,

$$d = f + p$$

F= effort delay or state effort, which depends on the complexity and fan-out of the gate. P=parasitic delay

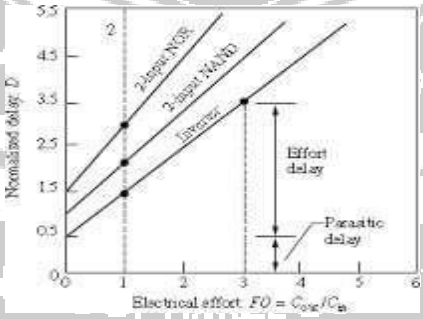

Fig 1.5.2: Normalized delay vs. fan-out

[Source: Neil H.E. Weste, David Money Harris —CMOS VLSI Design..]

Logical effort:

Logical effort is defined as the ratio of the input capacitance of the gate to the input capacitance of an inverter that delivers the same output current.

Parasitic delay:

Parasitic delay is defined as the delay of the gate when it drives zero load. This can be estimated with RC delay models. The inverter has 3 units of diffusion capacitance on the output.

Gate type	Number of input				
	1	2	3	4	n
INVERTER	1				
NAND		2	3	4	N
NOR		2	3	4	n
TRISTATE,MULTIPLEX	2	4	6	8	2

Logical effort and transistor sizing:

Logical effort provides a simple method to choose the best topology and number of stages of logic for a function. This quickly estimates the minimum possible delay for the given topology and to choose gate sizes that achieve this delay.

Delay in multistage logic networks:

Logical effort is independent of size and electrical effort is dependent on size.

1. path logical effort
2. path electrical effort
3. path effort
4. branching effort
5. path branching effort
6. path delay
7. minimum possible delay

Choosing the best number of stages:

Inverters can be added at the end of a path without changing its function. Extra inverters and parasitic delay, but do not change the path logical effort.

Device Modeling

SPICE provides a wide variety of MOS transistor models with various trade-offs between complexity and accuracy. Level 1 and Level 3 models were historically important, but they are no longer adequate to accurately model very small modern transistors. BSIM models are more accurate and are presently the most widely used. Some companies use their own proprietary models. This section briefly describes the main features of each of these models. It also describes how to model diffusion capacitance and how to run simulations in various process corners. The model descriptions are intended only as an overview of the capabilities and limitations of the models; refer to a SPICE manual for a much more detailed description if one is necessary.

Level 1 Models

The SPICE Level 1, or Shichman-Hodges Model [Shichman68] is closely related to the Shockley model described in EQ (2.10), enhanced with channel length modulation and the body effect. The basic current model is:

$$I_{ds} = \begin{cases} 0 & V_{gs} < V_t \quad \text{cutoff} \\ \mathrm{KP}\dfrac{W_{\mathrm{eff}}}{L_{\mathrm{eff}}}\left(1+\mathrm{LAMBDA}\times V_{ds}\right)\left(V_{gs}-V_t-V_{ds}/2\right)V_{ds} & V_{ds} < V_{gs}-V_t \quad \text{linear} \\ \dfrac{\mathrm{KP}}{2}\dfrac{W_{\mathrm{eff}}}{L_{\mathrm{eff}}}\left(1+\mathrm{LAMBDA}\times V_{ds}\right)\left(V_{gs}-V_t\right)^2 & V_{ds} > V_{gs}-V_t \quad \text{saturation} \end{cases}$$

The parameters from the SPICE model are given in ALL CAPS. Notice that is written instead as KP(*W*eff /*L*eff), where KP is a model parameter playing the role of *k. W*eff and *L*eff are the effective width and length). The LAMBDA term (LAMBDA = 1/*VA*) models channel length modulation The threshold voltage is modulated by the source-to- body voltage *Vsb* through the body effect.

The gate capacitance is calculated from the oxide thickness TOX. The default gate capacitance model in HSPICE is adequate for finding the transient response of digital circuits. More elaborate models exist that capture nonreciprocal effects that are important for analog design. Level 1 models are useful for teaching because they are easy to correlate with hand analysis, but are too simplistic for modern design.

Level 2 and 3 Models

The SPICE Level 2 and 3 models add effects of velocity saturation, mobility degradation, subthreshold conduction, and drain-induced barrier lowering. The Level 2 model is based on the Grove-Frohman equations, while the Level 3 model is based on empirical equations that provide similar accuracy, faster simulation times, and better convergence. However, these models still do not provide good fits to the measured I-V characteristics of modern transistors.

BSIM Models

The Berkeley Short-Channel IGFET1 Model (BSIM) is a very elaborate model that is now widely used in circuit simulation. The models

are derived from the underlying device physics but use an enormous number of parameters to fit the behavior of modern transistors. BSIM versions 1, 2, 3v3, and 4 are implemented as SPICE levels 13, 39, 49 and 54 respectively.

Features of the model include:

- Continuous and differentiable I-V characteristics across subthreshold, linear, and saturation regions for good convergence
- Sensitivity of parameters such as *Vt* to transistor length and width
- Detailed threshold voltage model including body effect and drain-induced barrier lowering
- Velocity saturation, mobility degradation, and other short-channel effects
- Multiple gate capacitance models
- Diffusion capacitance and resistance models
- Gate leakage models

As the BSIM models are so complicated, it is impractical to derive closed-form equations for propagation delay, switching threshold, noise margins, etc., from the underlying equations. However, it is not difficult to find these properties through circuit simulation. Device characterisation will show simple simulations to plot the device characteristics over the regions of operation that are interesting to most digital designers and to extract effective capacitance and resistance averaged across the switching transition. The simple RC model continues to give the designer important insight about the characteristics of logic gates.

Diffusion Capacitance Models

The p–n junction between the source or drain diffusion and the body forms a diode. We depends on the area and perimeter of the diffusion. HSPICE provides a number of methods to specify this geometry, controlled by the ACM (Area Calculation Method) parameter, which is

part of the transistor model. have seen that the diffusion capacitance determines the parasitic delay of a gate and The diffusion capacitance model is common across most device models including Levels 1–3 and BSIM. By default, HSPICE models use ACM = 0. In this method, the designer must specify the area and perimeter of the source and drain of each transistor.

The SPICE models also should contain parameters CJ, CJSW, PB, PHP, MJ, and MJSW. Assuming the diffusion is reverse-biased and the area and perimeter are specified, the diffusion capacitance between source and body is computed as described in

$$C_{sb} = \mathrm{AS} \times \mathrm{CJ} \times \left(1 + \frac{V_{sb}}{\mathrm{PB}}\right)^{-MJ} + \mathrm{PS} \times \mathrm{CJSW} \times \left(1 + \frac{V_{sb}}{\mathrm{PHP}}\right)^{-MJSW}$$

The drain equations are analogous, with S replaced by D in the model parameters. The BSIM3 models offer a similar area calculation model (ACM = 10) that takes into account the different sidewall capacitance on the edge adjacent to the gate. Note that the PHP parameter is renamed to PBSW to be more consistent.

$$C_{sb} = \mathrm{AS} \times \mathrm{CJ} \times \left(1 + \frac{V_{sb}}{\mathrm{PB}}\right)^{-MJ} + (\mathrm{PS} - W) \times \mathrm{CJSW} \times \left(1 + \frac{V_{sb}}{\mathrm{PBSW}}\right)^{-MJSW} + W \times \mathrm{CJSWG} \times \left(1 + \frac{V_{sb}}{\mathrm{PBSWG}}\right)^{-MJSWG}$$

If the area and perimeter are not specified, they default to 0 in ACM = 0 or 10, grossly underestimating the parasitic delay of the gate. HSPICE also supports ACM = 1, 2, 3, and 12 that provide nonzero default values when the area and perimeter are not specified. Check your models and read the HSPICE documentation carefully. The diffusion area and perimeter are also used to compute the junction leakage current. However, this current is

generally negligible compared to subthreshold leakage in modern devices.

Design Corners

Engineers often simulate circuits in multiple design corners to verify operation across variations in device characteristics and environment. HSPICE includes the .lib statement that makes changing libraries easy. The deck first sets SUP to the nominal supply voltage of 1.0 V. It then invokes .lib to read in the library specifying the TT conditions. In the stimulus, the. alter statement is used to repeat the simulation with changes. In this case, the design corner is changed. Altogether, three simulations are performed and three sets of waveforms are generated for the three design corners.