APPLICATION OF PLL

AM Demodulation:

A PLL may be used to demodulate AM signals as shown in the figure below. The PLL is locked to the carrier frequency of the incoming AM signal. The output of VCO which has the same frequency as the carrier, but unmodulated is fed to the multiplier. Since VCO output is always 90^0 before being fed to the multiplier. This makes both the signals applied to the multiplier and the difference signals, the demodulated output is obtained after filtering high frequency components by the LPF. Since the PLL responds only to the carrier frequencies which are very close to the VCO output, a PLL AM detector exhibits high degree of selectivity and noise immunity which is not possible with conventional peak detector type AM modulators.

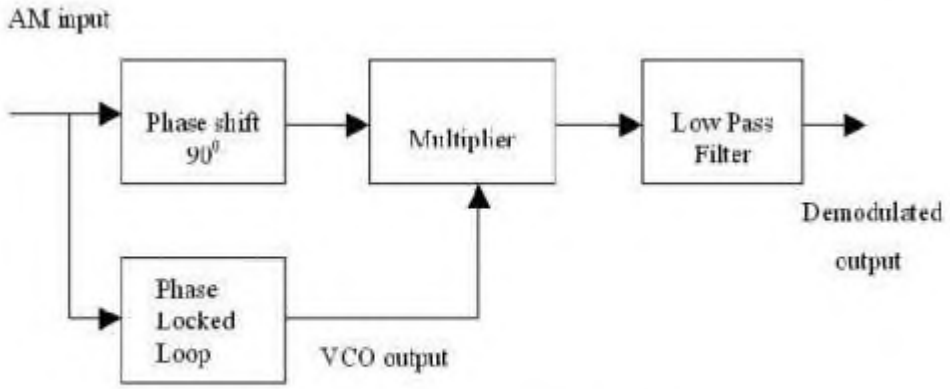
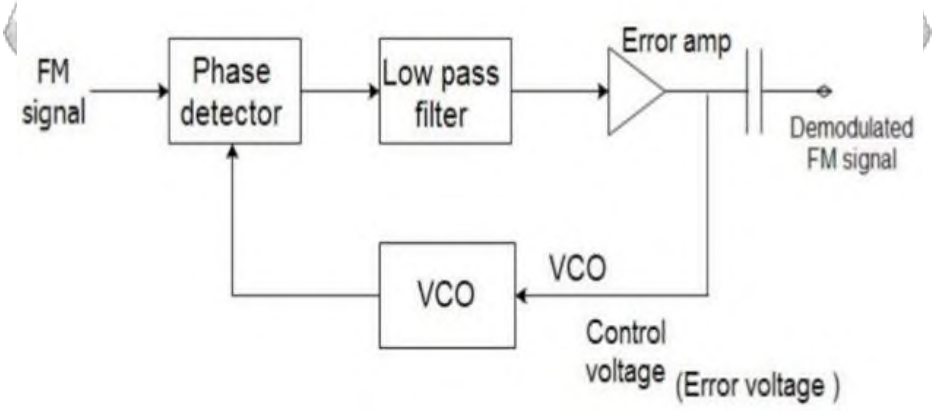


Fig. AM demodulator

FM Demodulation:

If PLL is locked to a FM signal, the VCO tracks the instantaneous frequency of the input signal. The filtered error voltage which controls the VCO and maintains lock with the input signal is the demodulated FM output.The VCO transfer characteristics determine the linearity of the demodulated output. Since, VCO used in IC PLL is highly linear, it is possible to realize highly linear FM demodulators.



FSK Modulation and Demodulation:

In digital data communication, binary data is transmitted by means of a carrier frequency. It uses two different carrier frequencies for logic 1 and logic 0 states of binary data signal. This type of data transmission is called **Frequency Shift Keying (FSK)**. In this data transmission, on the receiving end, two carrier frequencies are converted into 1 and 0 to get the original binary data. This process is called as **Frequency Shift Keying Demodulation**.

FSK Block Diagram:

A PLL can be used as a **Frequency Shift Keying Demodulator**, as shown in the Fig

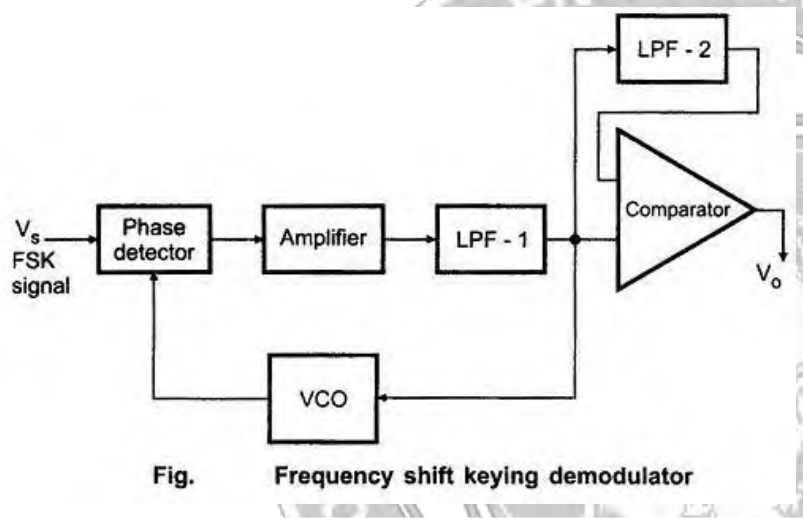


Fig. Frequency shift keying demodulator

It is similar to the PLL demodulator for analog FM signals except for the addition of a comparator to produce a reconstructed digital output signal. Let us consider that there are two frequencies, one frequency (f_1) is represented as "0" and other frequency (f_2) is represented as "1". If the PLL remain is locked into the FSK signal at both f_1 and f_2; the VCO control voltage which is also supplied to the comparator will be given as

$$V_{C1} = (f_1 - f_0) / K_v \text{ and}$$

$$V_{C2} = (f_2 - f_0) / K_v \text{ , respectively.}$$

where

- K_v is the voltage to frequency transfer coefficient of the VCO.

The difference between the two control voltage levels will be

$$\Delta V_C = (f_2 - f_1) / K_v.$$

The reference voltage for the comparator is derived from the additional low pass filter and it is adjusted midway between V_{C1} and V_{C2}.Therefore, for V_{C1} and V_{C2}, comparator gives output '0' and '1', respectively.

Frequency Synthesizer

The PLL can be used as the basis for frequency synthesizer that can produce a precise series of frequencies that are derived from a stable crystal controlled oscillator.

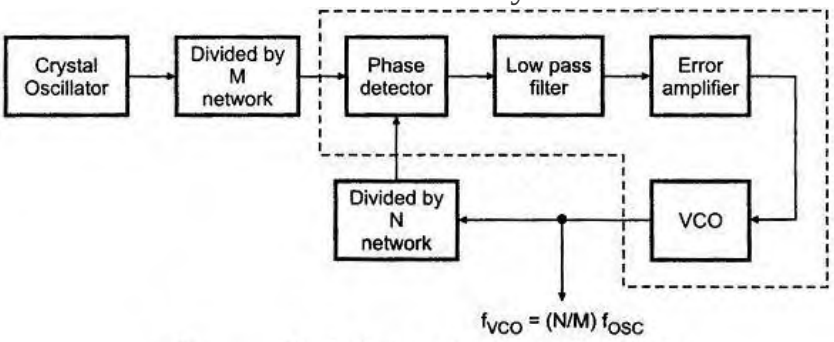


Fig. Block diagram of frequency synthesizer

The Fig. shows the Frequency Synthesizer Block Diagram. It is similar to frequency multiplier circuit except that divided by M network is added at the input of phase lock loop.The frequency of the crystal-controlled oscillator is divided by an integer factor M by divider network to produce a frequency f_{osc}/M

where

- f_{osc} is the frequency of the crystal controlled oscillator.

The VCO frequency f_{VCO} is similarly divided by factor N by divider network to give frequency equal to f_{vco} /N. When the PLL is locked in on the divided-down oscillator frequency, we will have $f_{osc}/M = f_{vco}/N$, so that $f_{vco}=(N/M)f_{osc}$.By adjusting divider counts to desired values large number of frequencies can be produced, all derived from the crystal controlled oscillator.

Operation of Basic Phase Locked Loop

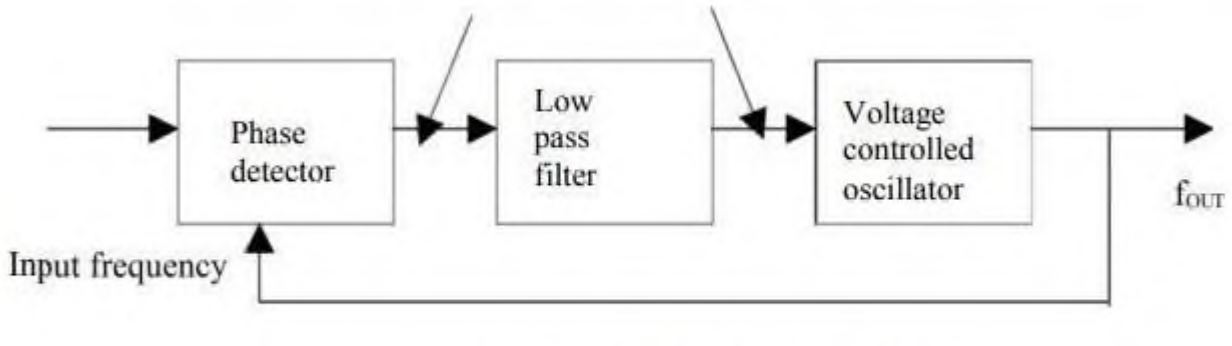


Fig Block diagram of PLL

The PLL consists of i) Phase detector ii) LPF iii) VCO. The phase detector or comparator compares the input frequency f_{IN} with feedback frequency f_{OUT}. The output of the phase detector is proportional to the phase difference between f_{IN} & f_{OUT}. The output of the phase detector is a dc voltage & therefore is often referred to as the error voltage. The output of the phase detector is then applied to the LPF, which removes the high frequency noise and produces a dc level. This dc level in turn, is input to the VCO. The output frequency of VCO is directly proportional to the dc level. The VCO frequency is compared with input frequency and adjusted until it is equal to the input frequencies.PLL goes through 3 states, i) free running ii) Capture iii) Phase lock.

Before the input is applied, the PLL is in free running state. Once the input frequency is applied the VCO frequency starts to change and PLL is said to be in the capture mode. The VCO frequency continuous to change until it equals the input frequency and the PLL is in phase lock mode. When Phase locked, the loop tracks any change in the input frequency through its repetitive action.

If an input signal vs of frequency fs is applied to the PLL, the phase detector compares the phase and frequency of the incoming signal to that of the output vo of the VCO. If the two signals differ in frequency of the incoming signal to that of the output vo of the VCO.The phase detector is basically a multiplier and produces the sum ($f_s + f_o$) and difference ($f_s - f_o$) components at its output.The high frequency component ($f_s + f_o$) is removed by the low pass filter and the difference frequency component is amplified then applied as control voltage v_c to VCO.

The signal v_c shifts the VCO frequency in a direction to reduce the frequency difference between fs and f_o. Once this action starts, we say that the signal is in the capture range. The VCO continues to change frequency till its output frequency is exactly the same as the input signal frequency. The circuit is then said to be locked. Once locked, the output frequency f_o of VCO is identical to fs except for a finite phase difference φ. This phase difference φ generates a corrective control voltage vc to shift the VCO frequency from f0 to

fs and thereby maintain the lock. Once locked, PLL tracks the frequency changes of the input signal. Thus, a PLL goes through three stages (i) free running, (ii) capture and (iii) locked or tracking.

Capture range: The range of frequencies over which the PLL can acquire lock with an input signal is called the capture range. This parameter is also expressed as percentage of fo.

Pull-in time: The total time taken by the PLL to establish lock is called pull-in time. This depends on the initial phase and frequency difference between the two signals as well as on the overall loop gain and loop filter characteristics.

Lock-in Range: Once the PLL is locked, It can track frequency changes in the incoming signals.The range of frequencies over which the PLL can maintain lock with the incoming signal is called the lock in range or tracking range.

Closed Loop Analysis of PLL:

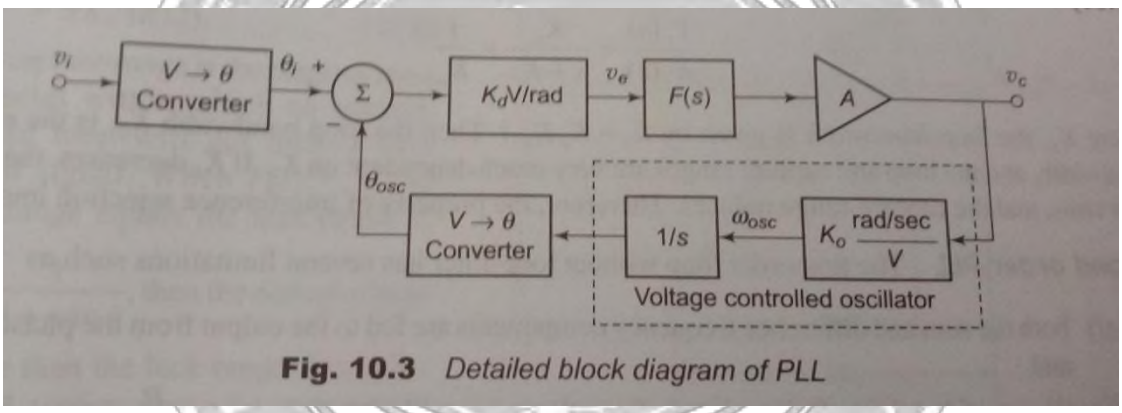


Fig. 10.3 *Detailed block diagram of PLL*

The i/p sinusoidal gain V_i is given as

$$V_i = V_p \sin(\omega t + \theta)$$

If the phase shift of the signal at the VCO o/p is θ_{osc},then the average value of the o/p of phase detector is

$$V_e = K_d(\theta_i - \theta_{osc})$$

$$where\ \theta_i\ \&\theta_{osc} \rightarrow phase\ shift$$

The phase of the signal at the o/p of VCO as a function of time is equal to integral of the VCO o/p frequency & can be expressed as

$$\omega_{osc(t)} = \frac{d\theta_{osc(t)}}{dt}$$

$$d\theta_{osc(t)} = \omega_{osc(t)} dt$$

$$\int d\theta_{osc(t)} = \int \omega_{osc(t)} dt + \theta_{osc\ at\ t=0}$$

$$\theta_{osc(t)} = \int \omega_{osc(t)} dt + \theta_{osc\ at\ t=0}$$

The integral component is represented as 1/S inside the VCO block. Oscillator frequency ω_{osc} & the dc control voltage V_c are related by

$$\omega_{osc} = \omega_c + K_o V_c$$

$$where,\ \omega_c \rightarrow centre\ or\ free\ running\ angular\ frequency,$$

$$that\ results\ when\ V_c = 0\ \&\ K_o\ is\ the\ VCO\ gain\ in\ rad/\sec\ per\ volt.$$

Then the closed loop transfer function of PLL

$$\frac{V_c(s)}{\theta_i(s)} = \frac{K_d F(S) A}{1 + K_d A F(S)\frac{K_o}{S}} = \frac{S K_d F(S) A}{S + K_d A F(S) K_o}$$

Response of the loop to frequency variation at i/p than phase.

$$\frac{V_c(s)}{\omega_i(s)} = \frac{V_c(S)}{S\theta_i(S)} = \frac{K_d F(S) A}{S + K_d A F(S) K_o}$$

$$\omega_i = \frac{d\theta_i}{dt}\ \&\ \omega_i(s) = s\theta_i(s)$$

F(S)=0,with the loop having a first order low pass frequency response.

$$\frac{V_c(s)}{\omega_i(s)} = \frac{K_v}{S + K_v} X \frac{1}{K_o}$$

$$K_v \rightarrow loop\ bandwidth.$$

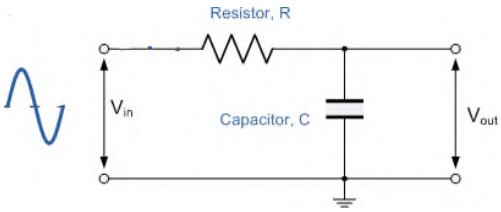
$$K_v = K_o K_d A$$

Second Order PLL:

The first order loop without loop-filter has several limitations.

1. Both the sum & difference frequency components are fed to the o/p from the phase detector.
2. All out-of band interfering signals from the i/p will appear shifted in frequency at the o/p.

The most common configuration of monolithic PLL in the second order loop with a loop –filter F(s) of a simple single-pole LPF realized with a resistor R & a Capacitor C in Fig

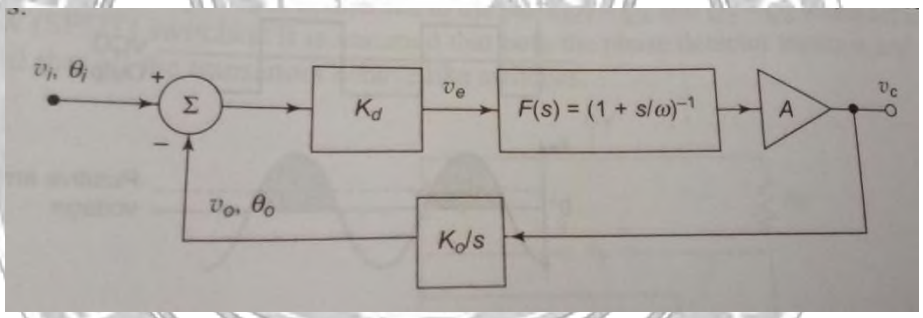


$$F(s) = \frac{1/SC}{R + 1/SC} = \frac{1}{1 + SRC}$$

$$= \frac{1}{1 + S/\omega} = \frac{1}{1 + Sr}$$

$$\omega = \frac{1}{RC} = \frac{1}{r}$$

The resulting block diagram of the second order PLL using single-pole loop filter.



Loop Lock-Range & Capture Range:

The loop lock-range is represented as the range of frequency about ω_o for which PLL maintains the relationship

$$\omega_i = \omega_{osc}$$

If the phase detector can determine the phase difference between θ_i & θ_{osc}

Over a $\pm\frac{\pi}{2}$ range ,then the lock-range is defined as

$$\omega_L = \pm \Delta m_{osc}$$

$$= K_d A K_o (\pm \frac{\pi}{2})$$

$$= \pm K_v (\frac{\pi}{2})$$

The capture range is the range of i/p frequencies with in which a initially unlocked loop will get locked with an i/p signal. When F(s)=1 ,the capture range equals the lock-range. If $F(S) = \frac{1}{1+S/m_i}$,then the capture range is smaller than the lock-range.