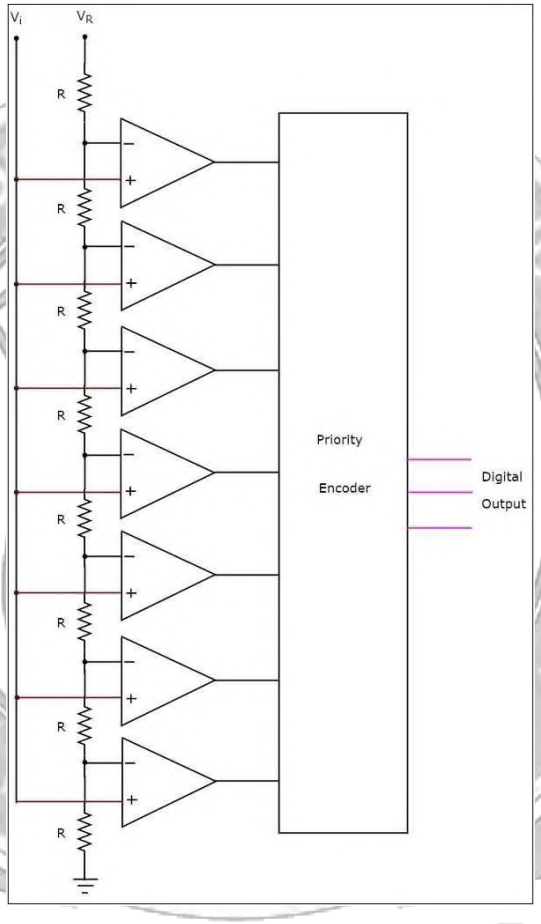
Types of ADC:

Flash Type ADC

Flash type ADC produces an equivalent digital output for a corresponding analog input in no time. Hence, flash type ADC is the fastest ADC.

The circuit diagram of a 3-bit flash type ADC is shown in the following figure −



The 3-bit flash type ADC consists of a voltage divider network, 7 comparators and a priority encoder.

The **working** of a 3-bit flash type ADC is as follows.

- The **voltage divider network** contains 8 equal resistors. A reference voltage VR is applied across that entire network with respect to the ground. The voltage drop across each resistor from bottom to top with respect to ground will be the integer multiples (from 1 to 8) of VR8VR8.
- The external **input voltage** Vi is applied to the non-inverting terminal of all comparators. The voltage drop across each resistor from bottom to top with respect to ground is applied to the inverting terminal of comparators from bottom to top.
- At a time, all the comparators compare the external input voltage with the voltage drops present at the respective other input terminal. That means, the comparison operations take place by each comparator **parallelly**.

- The **output of the comparator** will be '1' as long as Vi is greater than the voltage drop present at the respective other input terminal. Similarly, the output of comparator will be '0', when, Vi is less than or equal to the voltage drop present at the respective other input terminal.
- All the outputs of comparators are connected as the inputs of **priority encoder**.This priority encoder produces a binary code (digital output), which is corresponding to the high priority input that has '1'.
- Therefore, the output of priority encoder is nothing but the binary equivalent **(digital output)** of external analog input voltage, Vi.

The flash type ADC is used in the applications where the conversion speed of analog input into digital data should be very high.

Successive Approximation type ADC

Successive Approximation type ADC is the most widely used and popular ADC method. The conversion time is maintained constant in successive approximation type ADC, and is proportional to the number of bits in the digital output, unlike the counter and continuous type A/D converters. The basic principle of this type of A/D converter is that the unknown analog input voltage is approximated against an n-bit digital value by trying one bit at a time, beginning with the MSB. The principle of successive approximation process for a 4-bit conversion is explained here. This type of ADC operates by successively dividing the voltage range by half, as explained in the following steps.
(1) The MSB is initially set to 1 with the remaining three bits set as 000. The digital equivalent voltage is compared with the unknown analog input voltage.

(2) If the analog input voltage is higher than the digital equivalent voltage, the MSB is retained as 1 and the second MSB is set to 1. Otherwise, the MSB is set to 0 and the second MSB is set to 1. Comparison is made as given in step (1) to decide whether to retain or reset the second MSB.

The above steps are more accurately illustrated with the help of an example.
Let us assume that the 4-bit ADC is used and the analog input voltage is VA = 11 V. when the conversion starts, the MSB bit is set to 1.

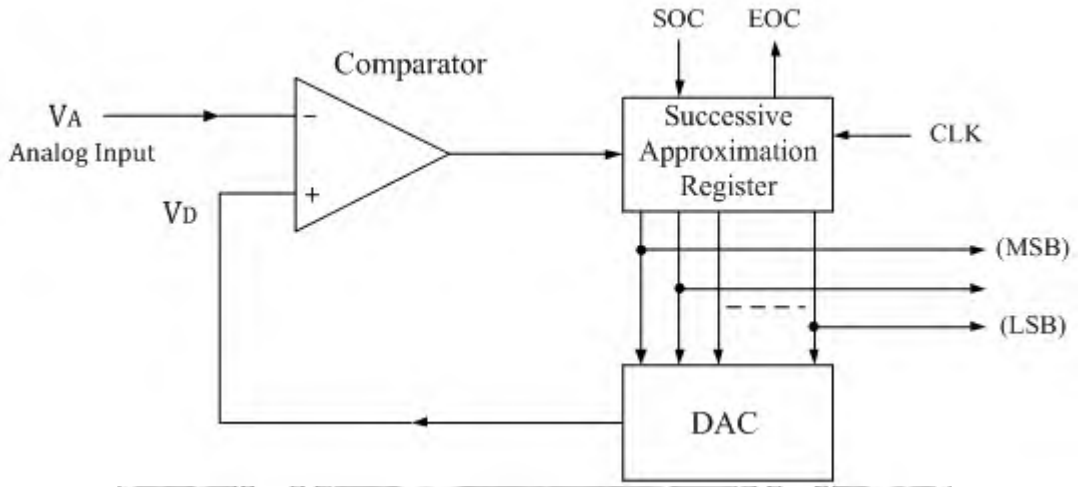
Now VA = 11V > VD = 8V = [1000]2

Since the unknown analog input voltage VA is higher than the equivalent digital voltage VD, as discussed in step (2), the MSB is retained as 1 and the next MSB bit is set to 1 as follows
VD = 12V = [1100]2

Now VA = 11V < VD = 12V = [1100]2
Here now, the unknown analog input voltage VA is lower than the equivalent digital voltage VD. As discussed in step (2), the second MSB is set to 0 and next MSB set to 1 as
VD = 10V = [1010]2

Now again VA = 11V > VD = 10V = [1010]2
Again as discussed in step (2) VA>VD, hence the third MSB is retained to 1 and the last bit

is set to 1. The new code word is
VD = 11V = [1011]2
Now finally VA = VD , and the conversion stops.
The functional block diagram of successive approximation type of ADC is shown below.



It consists of a successive approximation register (SAR), DAC and comparator. The output of SAR is given to n-bit DAC. The equivalent analog output voltage of DAC, VD is applied to the non-inverting input of the comparator. The second input to the comparator is the unknown analog input voltage VA. The output of the comparator is used to activate the successive approximation logic of SAR.When the start command is applied, the SAR sets the MSB to logic 1 and other bits are made logic 0, so that the trial code becomes 1000.

Advantages:

1. Conversion time is very small.
2. Conversion time is constant and independent of the amplitude of the analog input signal VA.

Disadvantages:

1 Circuit is complex.
2 The conversion time is more compared to flash type ADC.

Single Slope ADC

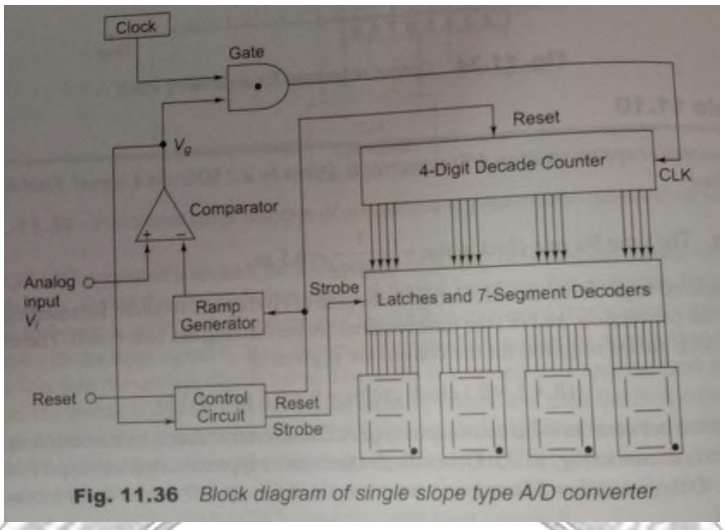


Fig. 11.36 *Block diagram of single slope type A/D converter*

These converter techniques are based on comparing the unknown analog i/p voltage with a reference voltage that begins at 0v & increases linearly with time.The time required for the reference voltage to reach the value of unknown analog i/p voltage is proportional to the amplitude of unknown analog i/p voltage.The time period can be measured using a digital counter.The main circuit of this converter is a ramp generator which on receiving a RESET from the control circuit increases linearly with time from 0v to a max volt Vm Assume a +ive analog i/p voltage Vi is applied at the non-inverting i/p of the comparator.When a RESET signal is applied to the control logic, the 4-digit decade counter resets to 0 & the ramp begins to increase.Vi is +ive the comparator o/p is in HIGH state.

This allows the clk pulse to pass to the i/p of the 4-digit counter through the AND gate & the counter is incremented.This process continues until the analog i/p voltage is greater than the ramp generator voltage.When the ramp generator voltage is equal to the analog i/p voltage, the comparator o/p becomes negatively saturated or logic 0.The clk is prevented from passing through the gate causing the counter operation.Then the control circuit generates a STROBE signal,which latches the counter values in the 4-digit latch,which is displayed on 7-segmant displays.The displayed value is then equivalent to the amplitude of analog input voltage.

Dual Slope ADC

The analog part of the circuit consists of a high input impedance buffer A_1,precision integrator A_2 and a voltage comparator.The converter first integrates the analog input signal V_a for a fixed duration of 2^n clk periods.Then it integrates an internal reference voltage VR of opposite polarity until the integrator output is zero.

Before the START command arrives,the switch SW_1 is connected to ground and SW_2 is closed.Any offset voltage present in the A_1,A_2,comparator loop after integration appears across the capacitor CAZ till the threshold of the comparator is achieved.The capacitor CAZ thus provides automatic compensation for the input-offset voltages of all the three amplifiers.

Later when SW2 opens,CAZ acts as a memory to hold the voltages required to keep the offset nulled. At the arrival of the START command at t=t1,the control logic opens SW_2 and connects to V_a and enables the counter starting from zero.The circuit uses an n-stage ripple counter and therefore the counter resets to zero after counting 2^n pulses.The analog voltage V_a is integrated for a fixed number 2^n counts of clk pulses after which the counter resets to zero.If the clock period is T the integration take place for a time $T=2^n$ x T and the output is a ramp going downwards.

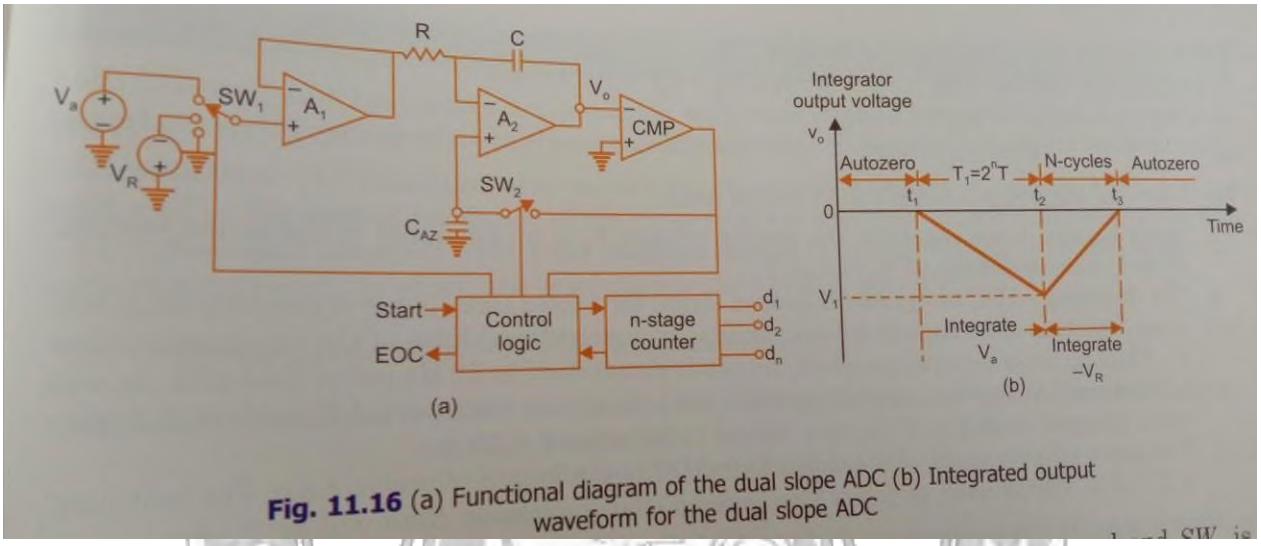


Fig. 11.16 (a) Functional diagram of the dual slope ADC (b) Integrated output waveform for the dual slope ADC

The counter resets itself to zero at the end of the integral T_1 and the switch SW_1 is connected to the refrence voltage $-V_R$. The output voltage Vo will now have a +ive slope.As long as V_o is –ive ,the output of the comparator is +ive and the control logic allows the clock pulse to be counted.When Vo become just zero at time $t=t_3$,the control logic issues an end of conversion(EOC) command and no further clock pulses enter the counter.

$$T_1 = t_2 - t_1 = \frac{2^n counts}{clock\ rate}$$

$$t_3 - t_2 = \frac{digital\ count\ N}{clock\ rate}$$

$$For\ an\ integrator, \Delta V_o = (-1/RC)V(\Delta t)$$

Voltage Vo will be equal to V1 at the instant t2 and can be given as

$$V_1 = (-1/RC)V_a(t_2 - t_1)$$

The voltage V1 is also given by

$$V_1 = (-1/RC)(-V_R)(t_2 - t_3)$$

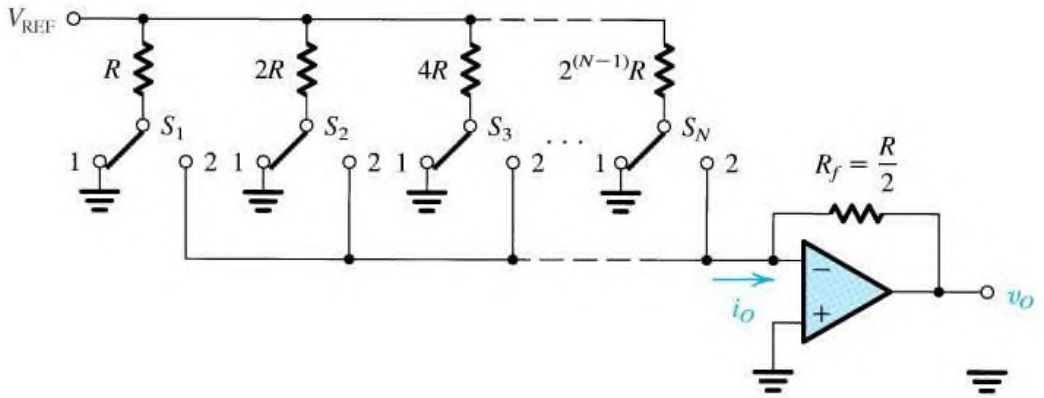
$$so, V_a(t_2 - t_1) = V_R(t_3 - t_2)$$

$$sub\ t_2 - t_1 = 2^n\ \&\ t_3 - t_2 = N$$

$$V_a(2^n) = V_R(N)$$

$$V_a = V_R(N/2^n)$$

Weighted Binary resistor DAC



Uses a summing amplifier with a binary weighted resistor network.Has n-electronic switches d1,d2,….dn controlled by binary input word.These switches are single pole double throw type.If the binary input to a particular switch is '1',it connects the resistance to the reference voltage ($-V_R$).If the input bit is '0',the switch connects to resistor to the ground.The output current Io for an ideal op-amp can be written as

$$I_o = I_1 + I_2 + I_3 + \cdots \ldots \ldots + I_n$$

$$I_o = I_1 + I_2 + I_3 + \cdots \ldots \ldots + I_n$$

$$I_o = \frac{V_R}{2R} d_1 + \frac{V_R}{2^2 R} d_2 + \cdots \ldots + \frac{V_R}{2^n R} d_n$$

$$I_o = \frac{V_R}{R} [d_1 2^{-1} + d_2 2^{-2} + \cdots .. + d_n 2^{-n}]$$

The o/p voltage

$$V_o = I_o R_f$$

$$= V_R \frac{R_f}{R} [d_1 2^{-1} + d_2 2^{-2} + \cdots .. + d_n 2^{-n}]$$

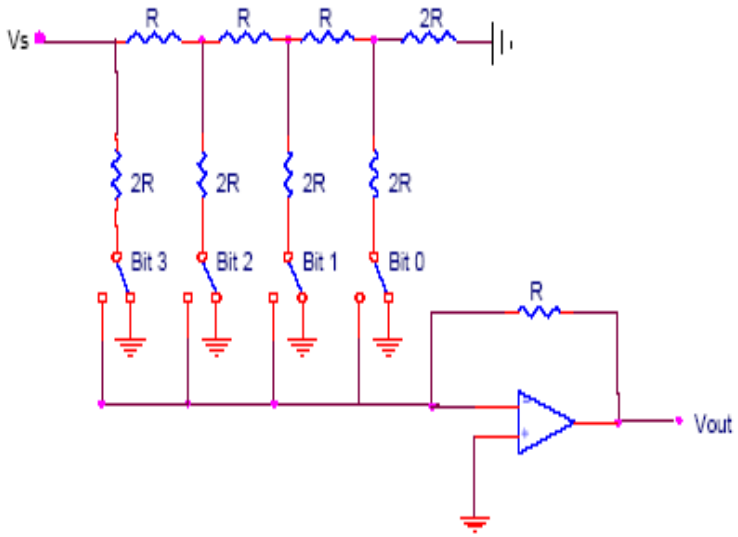
Advantage

- Easy principle/construction
- Fast conversion

Disadvantages

- Requirement of several different precise input resistor values: Requires large range of resistors (2048:1 for 12-bit DAC) with necessary high precision for low resistors one unique value per binary input bit. (High bit DACs)
- Larger resistors ~ more error.
- Precise large resistors – expensive.

R-2R Ladder DAC



Wide range of resistors are required in binary weighted resistor.This can be avoided by using R-2R ladder type DAC where only two values of resistors are required.The values of R ranges from 2.5kΩ to 10kΩ.Fig A the switch position d1,d2,d3 corresponds to the binary word 100. voltage at node C can be calculated by network analysis as

$$\frac{-V_R \frac{2}{3}R}{2R + \frac{2R}{3}} = \frac{-V_R}{4}$$

The output voltage is

$$V_o = \frac{-2R}{R}\left(-\frac{V_R}{4}\right) = \frac{V_R}{4} = \frac{V_{FS}}{2}$$

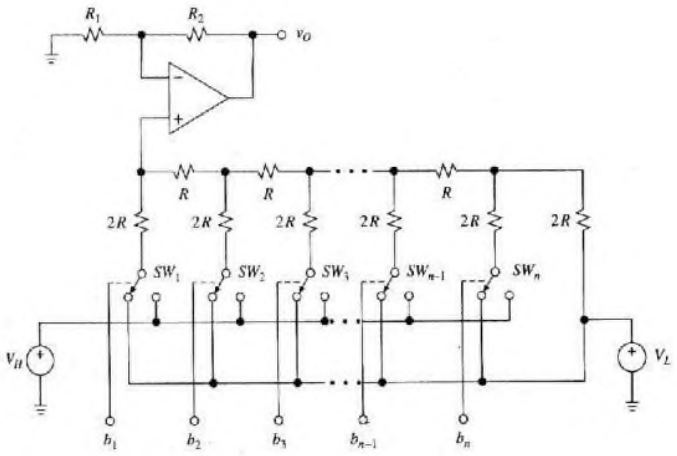
Advantages

- Only two resistor values
- Does not need as precision resistors as Binary weighted DACs
- Cheap and Easy to manufacture

Disadvantages

- Slower conversion rate

Voltage Mode R-2R Ladder Type D/A Converter



Voltage mode DAC

The arms of the ladder are switched between V_{ref} and ground.The o/p may be taken as a voltage.The expression for V_o can be obtained as

$$V_o = -\left(\frac{V_R}{R} X \frac{1}{2^n} X R_f\right) XD$$

$$where, V_o = feedback\ resistance\ of\ op-amp.$$

$$V_o = -I_{out} R_f$$

$$I_{out} = current\ resolution\ XD$$

$$V_o = -(current\ resolution\ XD) R_f$$

$$V_o = -(current\ resolution\ X R_f) D$$

The coefficient of D is the velocity resolution & can be called as simple resolution

$$V_o = -resolution\ XD$$

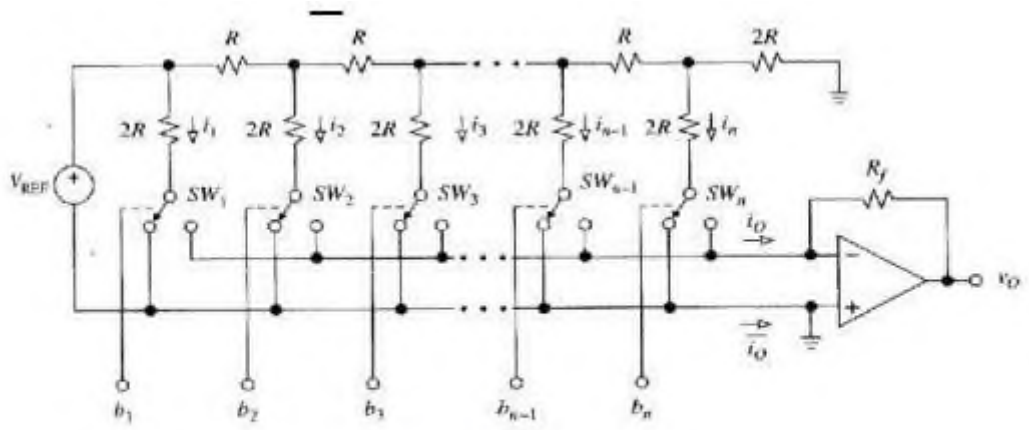
Resolution of R-2R ladder type DAC with voltage o/p is resolution

$$V_o = \left(\frac{1}{2^n} X \frac{VR}{R}\right) R_f$$

Advantages

1. The major advantage of this technique is that it allows us to interpolate between any two voltages, neither of which need not be a zero.
2. More accurate selection and design of resistors R and 2R are possible and simple construction.
3. The binary word length can be easily increased by adding the required number or R-2R sections.

Inverted R-2R Ladder (Current Mode R-2R Ladder)



Current mode DAC

In weighted resistor type DAC & R-2R ladder type DAC, current flowing in the resistors changes as the i/p changes.More power dissipation causes heating which in turn causes non-linearity in DAC.This can be avoided completely in Inverted R-2R ladder type DAC.A 3-bit inverted R-2R ladder type DAC where the position of MSB & LSB is interchanged.In fig when switch di is at logical 0 *ie,* to the left the current through 2R resistor flows the ground .When the switch di is at logical 1 *ie,* to the right the current through 2R sinks to the virtual ground.The current divides equally at each of the nodes.This is because the equivalent resistance to the right or to the left at any node is exactly 2R.

Advantages

1. The major advantage of current mode D/A converter is that the voltage change across each switch is minimal. So the charge injection is virtually eliminated and the switch driver design is made simpler.
2. In Current mode or inverted ladder type DACs, the stray capacitance do not affect the Speed of response of the circuit due to constant ladder node voltages. So improved speed performance.