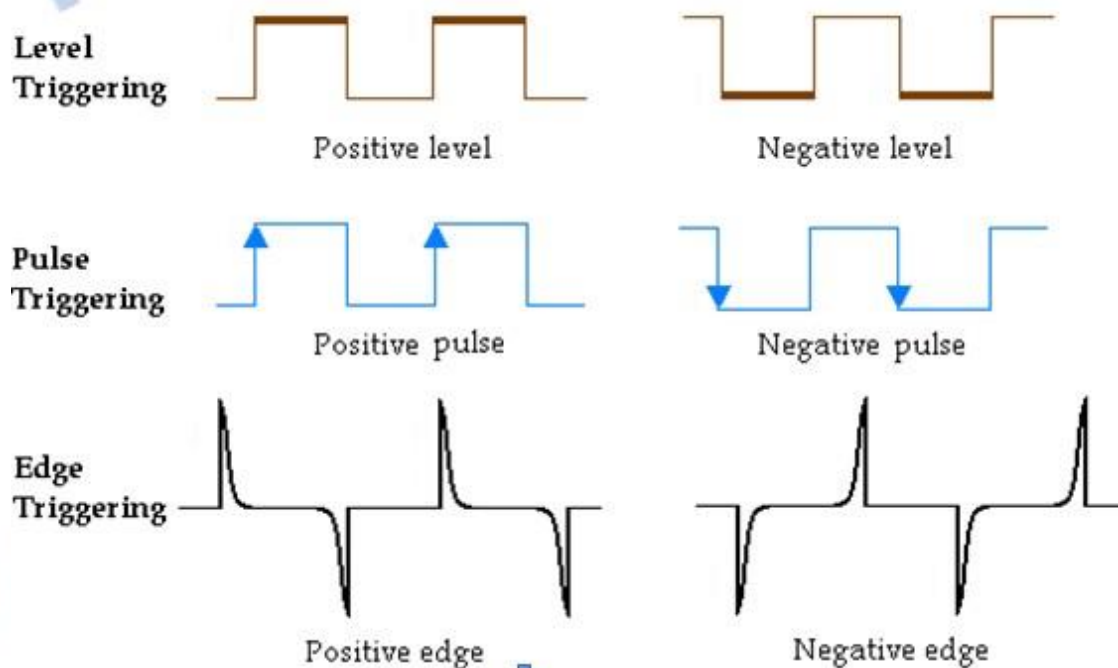


## 2. TRIGGERING OF FLIP-FLOPS

The state of a Flip-Flop is switched by a momentary change in the input signal. This momentary change is called a trigger and the transition it causes is said to trigger the Flip-Flop. Clocked Flip-Flops are triggered by pulses. A clock pulse starts from an initial value of 0, goes momentarily to 1 and after a short time, returns to its initial 0 value.

Latches are controlled by enable signal, and they are level triggered, either positive level triggered or negative level triggered. The output is free to change according to the S and R input values, when active level is maintained at the enable input.



## EDGE TRIGGERED FLIP-FLOPS

Flip-Flops are synchronous bistable devices (has two outputs Q and Q'). In this case, the term synchronous means that the output changes state only at a specified point on the triggering input called the clock (CLK), i.e., changes in the output occur in synchronization with the clock.

An *edge-triggered Flip-Flop* changes state either at the positive edge (rising edge) or at the negative edge (falling edge) of the clock pulse and is sensitive to its inputs only at this transition of the clock. The different types of edge-triggered Flip-Flops are—

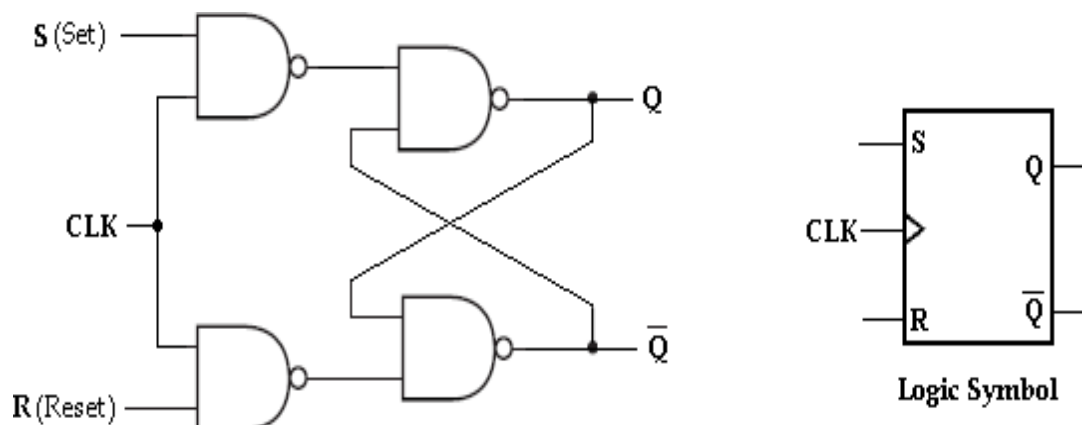
S-R Flip-Flop (Set - Reset) J-K  
Flip-Flop (Jack Kilby) D Flip-  
Flop (Delay)  
T Flip-Flop (Toggle)

Although the S-R Flip-Flop is not available in IC form, it is the basis for the D and J-K Flip-Flops. Each type can be either positive edge-triggered (no bubble at C input) or negative edge-triggered (bubble at C input).

The key to identifying an edge-triggered Flip-Flop by its logic symbol is the small triangle inside the block at the clock (C) input. This triangle is called the **dynamic input indicator**.

### S-R Flip-Flop

The S and R inputs of the S-R Flip-Flop are called *synchronous* inputs because data on these inputs are transferred to the Flip-Flop's output only on the tri edge of the clock pulse. The circuit is similar to SR latch except enable signal is replaced by clock pulse (CLK). On the positive edge of the clock pulse, the circuit responds to the S and R inputs.



**SR Flip-Flop**

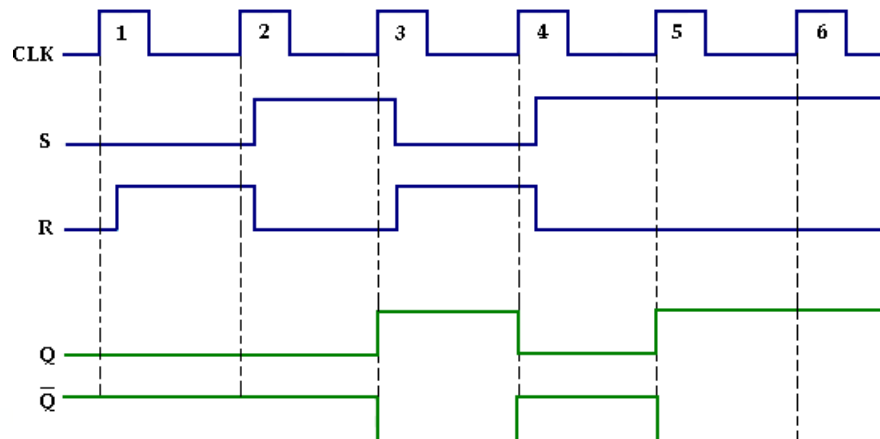
When S is HIGH and R is LOW, the Q output goes HIGH on the triggering edge of the clock pulse, and the Flip-Flop is SET. When S is LOW and R is HIGH, the Q output goes LOW on the triggering edge of the clock pulse, and the Flip-Flop is RESET. When both S and R are LOW, the output does not change from its prior state. An invalid condition exists when both S and R are HIGH.

CLK	S	R	Q <sub>n</sub>	Q <sub>n+1</sub>	State
1	0	0	0	0	No Change (NC)
1	0	0	1	1	
1	0	1	0	0	Reset
1	0	1	1	0	
1	1	0	0	1	Set
1	1	0	1	1	
1	1	1	0	x	Indeterminate *
1	1	1	1	x	

**Truth table for SR Flip-Flop**

The timing diagram of positive edge triggered SR flip-flop is shown below.

**Input and output waveforms of SR Flip-Flop**



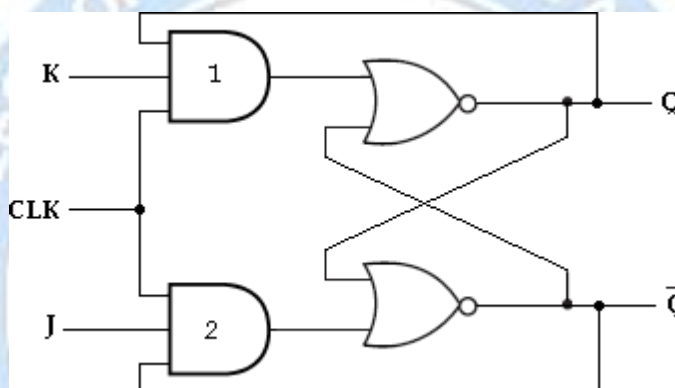
The characteristic table for JK Flip-Flop is shown in the table below. From the table, K-map for the next state transition ( $Q_{n+1}$ ) can be drawn and the simplified logic expression which represents the characteristic equation of JK Flip-Flop can be found.

S	R	$Q_n$	$Q_{n+1}$
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	x
1	1	1	x

### J-K Flip-Flop:

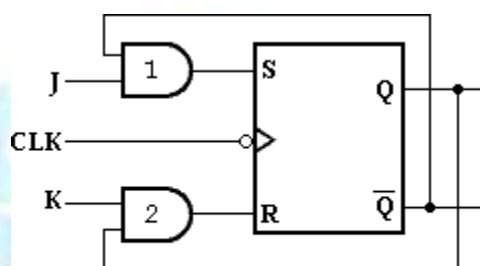
JK means Jack Kilby, Texas Instrument (TI) Engineer, who invented IC in 1958.

JK Flip-Flop has two inputs J(set) and K(reset). A JK Flip-Flop can be obtained from the clocked SR Flip-Flop by augmenting two AND gates as shown below.

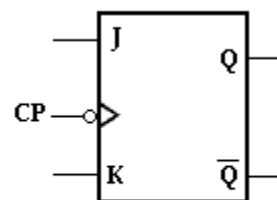


**JK Flip Flop**

The data input J and the output Q' are applied to the first AND gate and its output (JQ') is applied to the S input of SR Flip-Flop. Similarly, the data input K and the output Q are applied to the second AND gate and its output (KQ) is applied to the R input of SR Flip-Flop.



**(a) Using SR flipflop**



**(b) Graphic symbol**

$$J = K = 0$$



When  $J=K= 0$ , both AND gates are disabled. Therefore clock pulse have no effect, hence the Flip-Flop output is same as the previous output.

**J= 0, K= 1**

When  $J= 0$  and  $K= 1$ , AND gate 1 is disabled i.e.,  $S= 0$  and  $R= 1$ . This condition will reset the Flip-Flop to 0.

**J= 1, K= 0**

When  $J= 1$  and  $K= 0$ , AND gate 2 is disabled i.e.,  $S= 1$  and  $R= 0$ . Therefore the Flip-Flop will set on the application of a clock pulse.

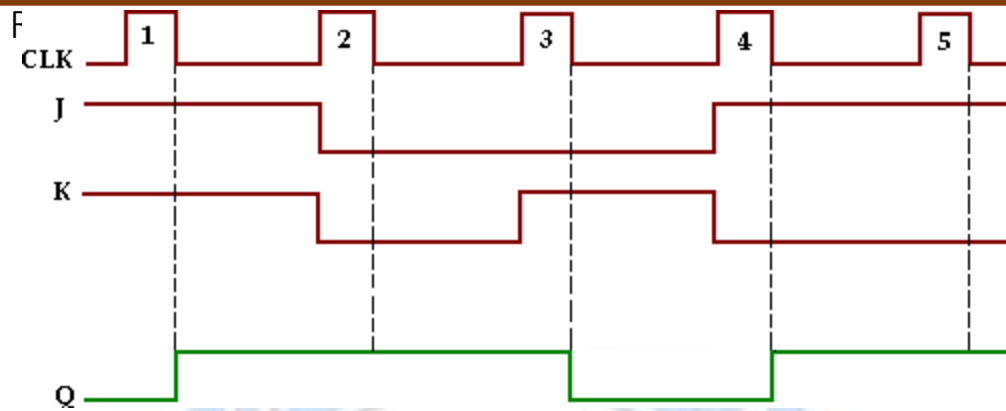
**J= K= 0**

When  $J=K= 1$ , it is possible to set or reset the Flip-Flop. If  $Q$  is High, AND gate 2 passes on a reset pulse to the next clock. When  $Q$  is low, AND gate 1 passes on a set pulse to the next clock. Eitherway,  $Q$  changes to the complement of the last state i.e., toggle. Toggle means to switch to the opposite state.

**Truth table**

CLK	Inputs		Output	State
	J	K	$Q_{n+1}$	
1	0	0	$Q_n$	No Change
1	0	1	0	Reset
1	1	0	1	Set
1	1	1	$Q_n'$	Toggle

The timing diagram of negative edge triggered JK flip-flop is shown below



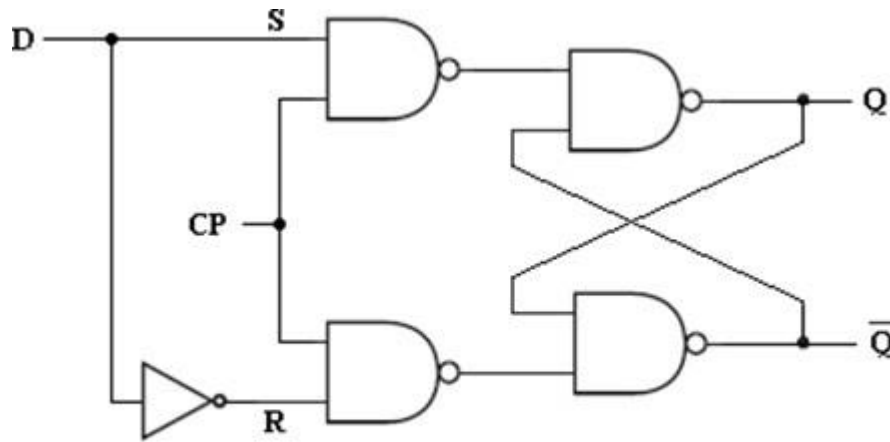
**Input and output waveforms of JK Flip-Flop**

### Characteristic table and Characteristic equation:

The characteristic table for JK Flip-Flop is shown in the table below. From the table, K-map for the next state transition ( $Q_{n+1}$ ) can be drawn and the simplified logic expression which represents the characteristic equation of JK Flip-Flop can be found.

### D Flip-Flop:

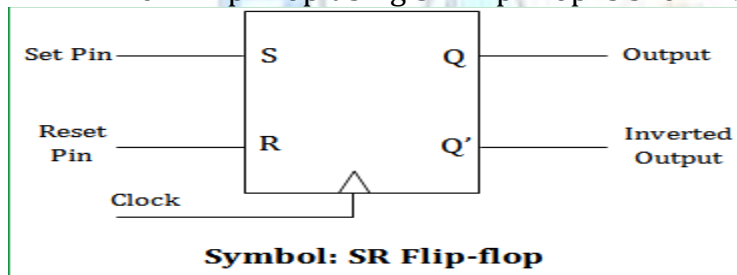
Like in D latch, in D Flip-Flop the basic SR Flip-Flop is used with complemented inputs. The D Flip-Flop is similar to D-latch except clock pulse is used instead of enable input.



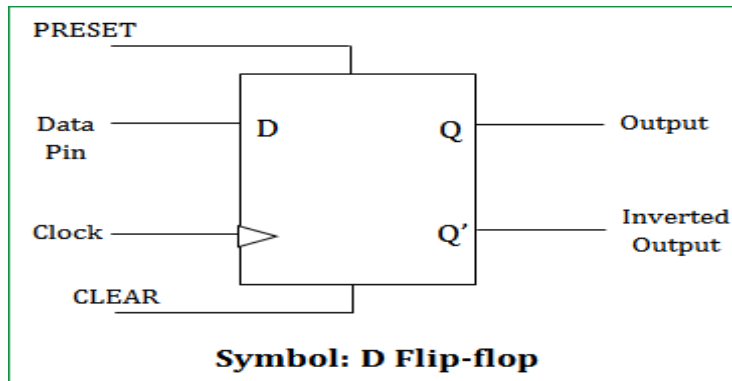
### D Flip-Flop

To eliminate the undesirable condition of the indeterminate state in the RS Flip-Flop is to ensure that inputs S and R are never equal to 1 at the same time. This is done by D Flip-Flop. The D (*delay*) Flip-Flop has one input called delay input and clock pulse input.

The D Flip-Flop using SR Flip-Flop is shown below.







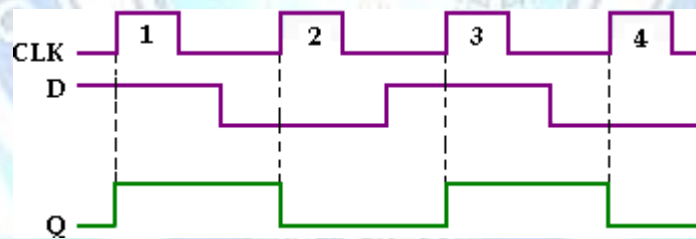
**Truth Table:**

The truth table of D Flip-Flop is given

1	0	0	Reset
1	1	1	Set
0	x	$Q_n$	No Change

**Truth table for D Flip-Flop**

The timing diagram of positive edge triggered D flip-flop is shown below.



**Input and output waveforms of clocked D Flip-Flop**

Looking at the truth table for D Flip-Flop we can realize that  $Q_{n+1}$  function follows the D input at the positive going edges of the clock pulses

**Characteristic table and Characteristic equation:**

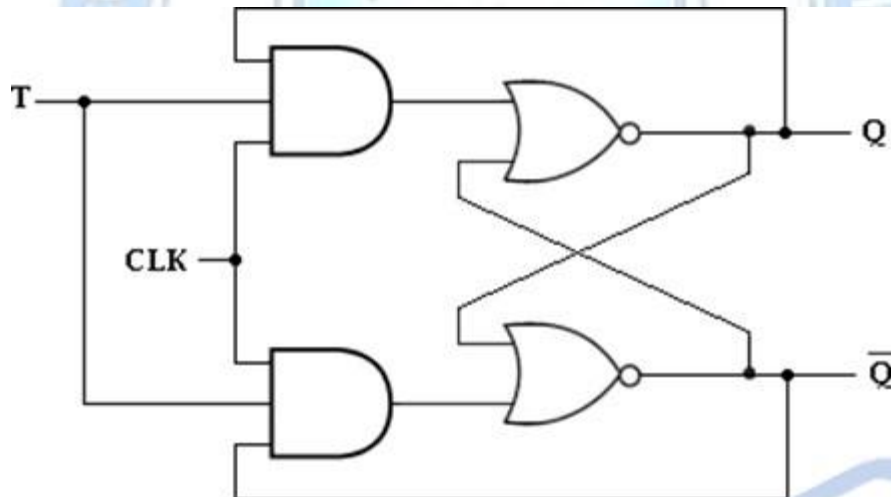
The characteristic table for D Flip-Flop shows that the next state of the Flip-Flop is independent of the present state since  $Q_{n+1}$  is equal to D. This means that an input pulse will transfer the value of input D into the output of the Flip-Flop independent of the value of the output before the pulse was applied.

The characteristic equation is derived from K-map.

$Q_n$	$D$	$Q_{n+1}$
0	0	0
0	1	1
1	0	0
1	1	1

### T Flip-Flop

The T (*Toggle*) Flip-Flop is a modification of the JK Flip-Flop. It is obtained from JK Flip-Flop by connecting both inputs J and K together. Regardless of the present state, the Flip-Flop complements its output when the clock pulse occurs while input T= 1.



**T Flip-Flop**

When  $T = 0$ ,  $Q_{n+1} = Q_n$ , i.e., the next state is the same as the present state and no change occurs.

When  $T = 1$ ,  $Q_{n+1} = Q_n'$ , i.e., the next state is the complement of the present state.

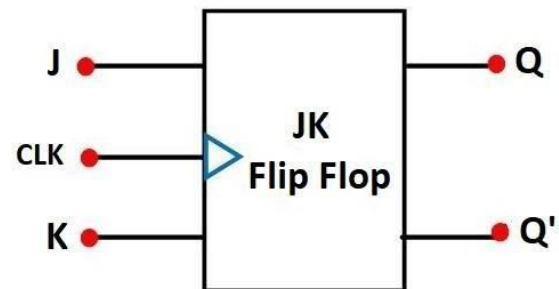
## T Flip-Flop to D Flip-Flop

The excitation table for the above conversion is

Input	Present state	Next state	Flip-Flop Input
D	$Q_n$	$Q_{n+1}$	T
0	0	0	0
0	1	0	1
1	0	1	1
1	1	1	0

## Truth Table of JK Flip Flop

C	J	K	Q	Q'
HIGH	0	0	Latch	Latch
HIGH	0	1	0	1
HIGH	1	0	1	0
HIGH	1	1	Toggle	Toggle
LOW	0	0	Latch	Latch
LOW	0	1	Latch	Latch
LOW	1	0	Latch	Latch
LOW	1	1	Latch	Latch



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