JFET OPERATIONAL AMPLIFIER:

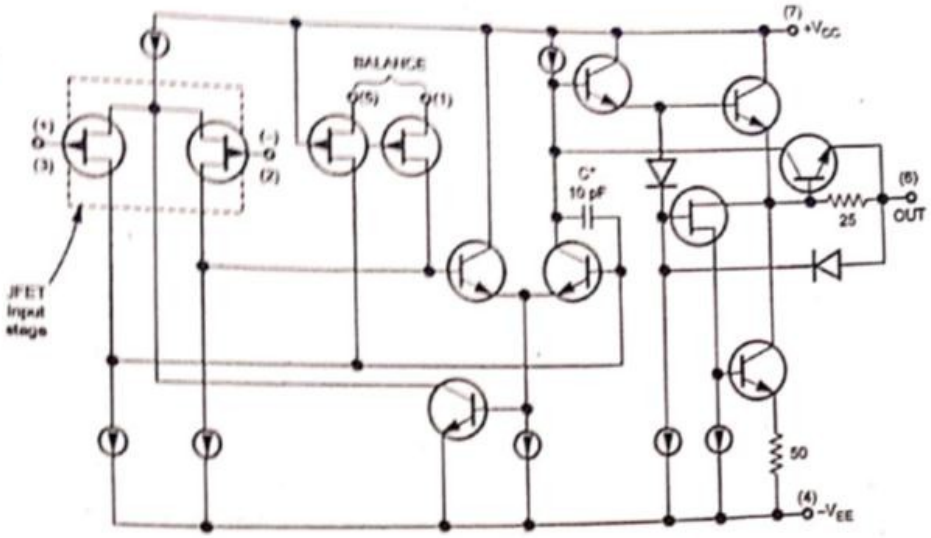
LF155 JFET OP-AMP:

The input impedance of the op-amp increased by using JFET differential amplifier as its input stage**.** It is the first monolithic JFET which uses well matched high voltage JFETs on the same chip with standard bipolar transistors. It has offset adjust feature due to which drifts and CMRR do not degrade.

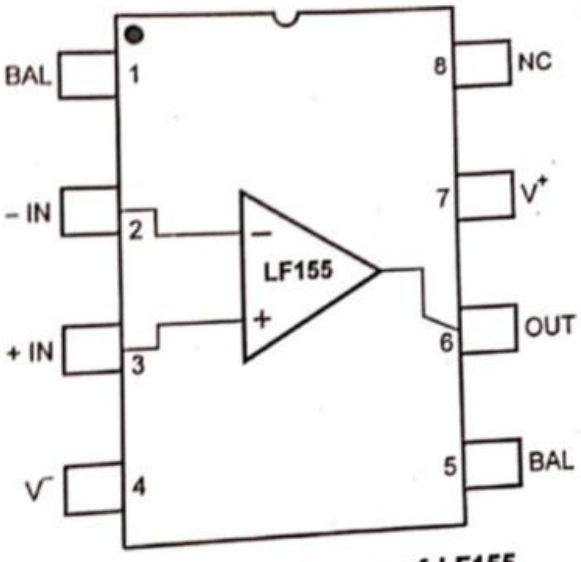
Features:

- Guaranteed Offset Voltage Drift on All Grades.
- Guaranteed Slew Rate on All Grades.
- Guaranteed Low Input Offset Current 10pA Max.
- Guaranteed Low Input Bias Current 50pA Max.
- Guaranteed High Slew Rate (156A/356A) 10V/µs Min.
- Fast Settling to 0.01% 1.5µS.

Internal Schematic:



Schematic of LF155



Pin diagram of LF155

Applications:

- Precision high speed integrators
- Fast D/A and A/D converters
- High impedance buffers Wideband, low noise, low drift amplifiers
- Logarithmic amplifiers

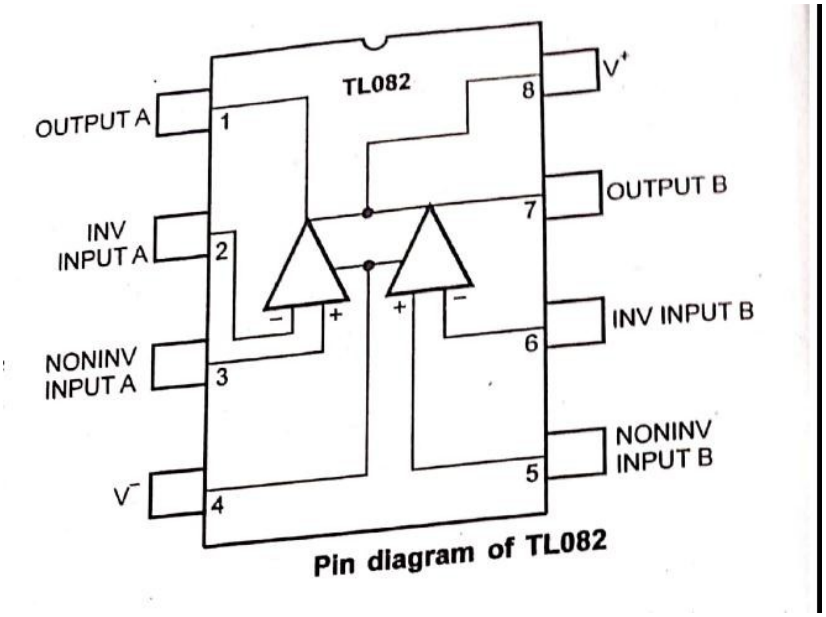
TL082 JFET op-amp:

The op-amp TL082 is low cost, high speed, dual JFET input op-amp with an internally trimmed input offset voltage.JFET has large reverse breakdown voltages from gate to source and drain hence clamping across the inputs is not required. This large differential input voltages can easily be accommodated without the need of large supply current.This op-amp requires low supply current and still maintain high slew rate and large gain bandwidth product. Due to JFET input stage,the input bias current and offset current is very low.

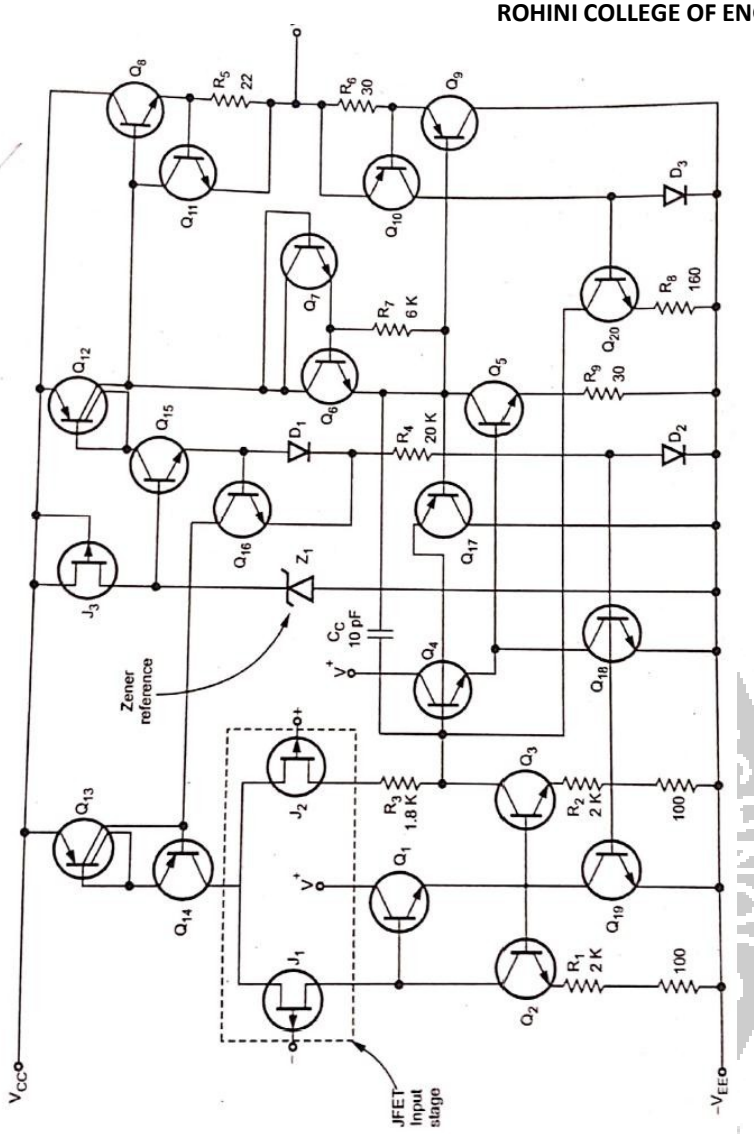
FEATURES

- Internally Trimmed Offset Voltage: 15 mV
- Low Input Bias Current: 50 pA
- Low Input Noise Voltage: 16nV/√Hz
- Low Input Noise Current: 0.01 pA/√Hz
- Wide Gain Bandwidth: 4 MHz
- High Slew Rate: 13 V/µs
- Low Supply Current: 3.6 mA
- High Input Impedance: 1012Ω
- Low Total Harmonic Distortion: ≤0.02%
- Low 1/f Noise Corner: 50 Hz
- Fast Settling Time to 0.01%: 2 µs

Internal Schematic:



Pin diagram of TL082



Internal schematic of TL082