ASIC DESIGN FLOW

An ASIC is classified into

1. Full custom ASIC
2. Semi custom ASIC

Full Custom ASIC:

- Full custom includes all possible logic cells and mask layers that are customized.
- These are very expensive to manufacture and design.
- Example is microprocessor.
- In full custom ASIC an engineer design some or all logic cells ,circuits, or layout specifically for one ASIC.

Semi Custom ASIC:

- In semicustom asic all the logic cells are predesigned and some of the mask layers are customized. The types of semicustom ASIC are

1. Standard cell based ASIC
2. Gate array based ASIC

1. Standard cell based ASIC:-

- A cell based ASIC or cell based IC (CBIC) uses predesigned logic cells like AND gates, OR gates, multiplexers, Flipflops.
- The predefined logic cells are known as standard cells. The standard cell areas are called flexible blocks
- The flexible blocks used in combination with larger predesigned cells, like micro controllers and micro processors, these are called mega cells.

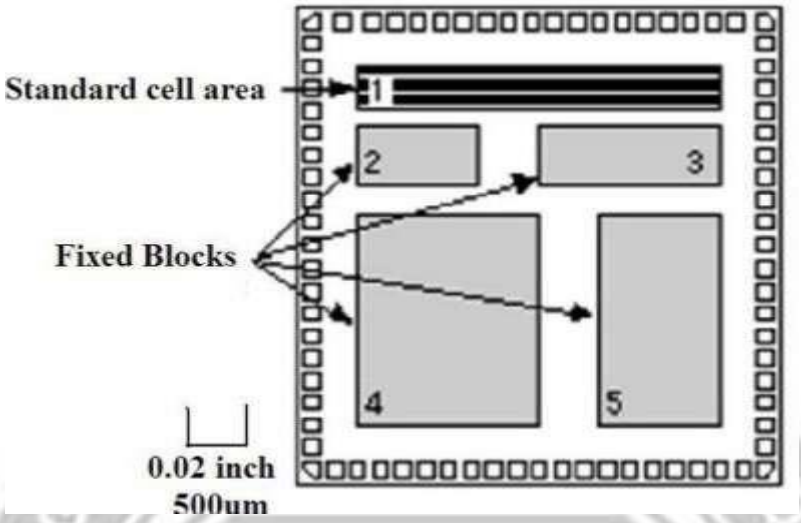

Fig 5.5.1: Cell based ASIC Advantages

[Source: R.Jacob Baker, Harry W.LI., David E.Boyee, ―CMOS Circuit Design, Layout and Simulation]

- Less cost
- Less time
- Reduced Risk
- Transistor operates at maximum speed.

Disadvantages:

- Expense of designing standard cell library is high
- Time needed to fabricate all layers for each new design is high.

2. Gate array based ASIC

- Gate array (GA) based ASIC has predefined transistors on the silicon wafer. The predefined pattern of transistors on a gate array is the base array. The base array is made up of a smallest element called primitive cell.
- To distinguish this type of gate array from other types of gate array ,this is often called MASKED GATE ARRAY.(MGA)

- MACROS: the logic cells in a gate array library are called macro.
- The types of MGA or gate array based ASIC are

1. Channeled gate array
2. Channel less gate array
3. Structured gate array

Channeled Gate Array:

- Channeled gate array has space between the rows of transistor for wiring
- Features:

1. Only the interconnect is customized.
2. Interconnect uses predefined spaces between rows of base cells.
3. Manufacturing lead time is between two days and two weeks.

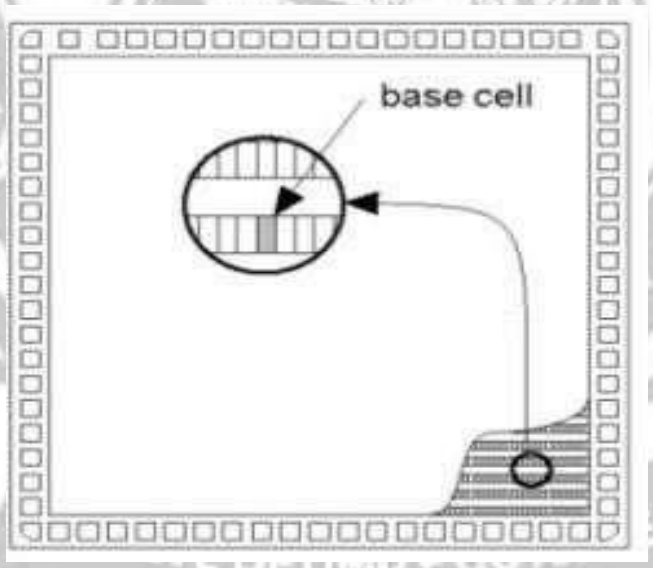

Fig 5.5.2: Channeled Gate Array

[Source: R.Jacob Baker, Harry W.LI., David E.Boyee, ―CMOS Circuit Design, Layout and Simulation]

- It is also known as channel free gate array.
- The routing on a channel less gate array uses rows of unused transistors.
- Features:

4. Top few mask layers are customized interconnect.
5. Manufacturing lead time is between two days and two weeks

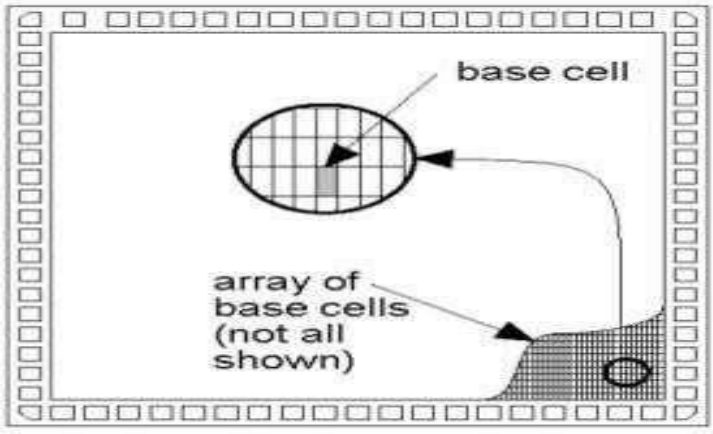

Fig 5.5.3: Channel less Gate Array

[Source: R.Jacob Baker, Harry W.LI., David E.Boyee, ―CMOS Circuit Design, Layout and Simulation]

6. Structured Gate Array:

- It can be either channeled or channel less, but it includes custom block.
- It is also known as master slice or master image
- This embedded area either contains a different base cell that is more suitable for building memory cells.

Features:

1. only the interconnect is customized
2. Custom blocks can be embedded.
3. Manufacturing lead time is between two days and two weeks.

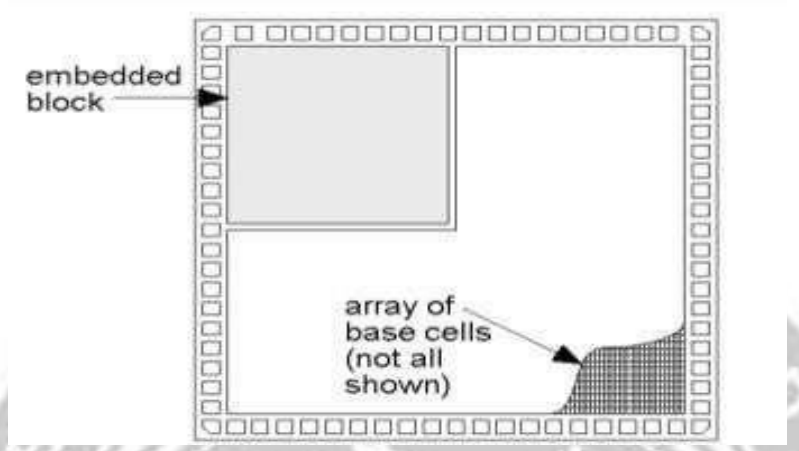

Fig 5.5.4: Structured Gate Array Advantages

[Source: R.Jacob Baker, Harry W.LI., David E.Boyee, ―CMOS Circuit Design, Layout and Simulation]

1. Improved area efficiency
2. Increased performance
3. Lower cost
4. Faster turn around

Disadvantage:

Embedded function is fixed.

Programmable ASIC:

- In which all the all the logic cells are predesigned and none of the mask layers are customized.
- The two types are

1. Programmable logic device
2. Field programmable gate array

Programmable logic device: (PLD)

- Programmable logic devices are standard IC and available in standard configuration .PLD may be configured or programmed.

Features:

1. No customized mask layers or logic cells.
2. Fast design turnaround
3. Single large block of programmable interconnect
4. Matrix of large macro cells

Field programmable gate array: (FPGA)

- Complex PLD's are called FPGA.
- FPGA are growing rapidly and replace TTL in microelectronic system

Characteristics:

1. No mask layers are customized.
2. Programming basic logic cells and interconnects.
3. Core with regular array of programmable basic logic cells that implement combinational and sequential logic.
4. Matrix of programmable interconnect surrounds the basic logic cells.
5. Programmable I/O cells surround the core.
6. Design turnaround is few hours.

ASIC Design Flow Steps of logic design:

Step1: Design entry

Enter the design into an ASIC design systems ,either using a HDL or schematic

entry

Step 2.Logic synthesis

Use VHDL or verilog and a logic synthesis tool to produce a netlist.

Step 3: System portioning

Divide a large system into an ASIC sized pieces.

Step 4: Pre-layout simulation

check whether design function are correct.

Steps of physical design:

Step 5: Floor planning

Arrange the blocks of the netlist on the chip.

Step 6: Placement:

Decide the locations of cells in a block.

Step 7: Routing:

Make the connections between cells and blocks.

Step 8.Extraction:

Determine the resistance and capacitance of the interconnect.

Step 9: Post layout simulation:

Check to see design still works with the added loads.

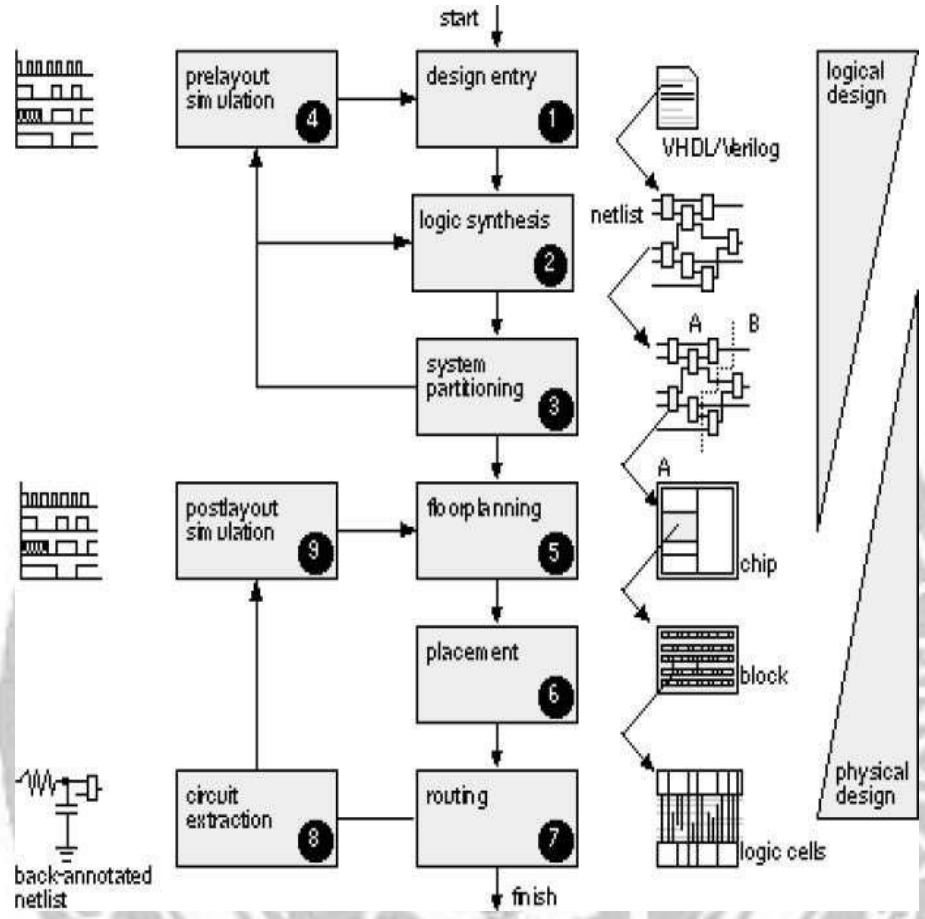

Fig 5.5.5: ASIC Cell Library

[Source: R.Jacob Baker, Harry W.LI., David E.Boyee, ―CMOS Circuit Design, Layout and Simulation]

ASIC cell library

- Cell library is very important in ASIC design.
- For MGA and CBIC there are three choices to have the cell library.

i. ASIC manufacturer will supply a cell library.

ii. Cell library is bought from a third party library vendor.

iii. Build our own library.

Customer owned tooling:

- If an ASIC design is completed using cell library we own the mask that is used to manufacture the ASIC. This is called Customer owned tooling. Each cell in an ASIC cell library contain the following,

1. Physical layout
2. Behavioral model
3. verilog/VHDL model
4. Timing model
5. Test strategy
6. Circuit schematic
7. Cell icon
8. Wire load model
9. Routing model