# UNIT-I

# COMBINATIONAL LOGIC

Combinational circuits-Karnaugh Map-Analysis and Design Procedures-Binary Adder-Subtractor-Decimal Adder- Magnitude comparator-Decoder-Encoder-Multiplexers-Demultiplexers.

## INTRODUCTION:

The logic circuits for digital systems may be either Combinational or Sequential circuits

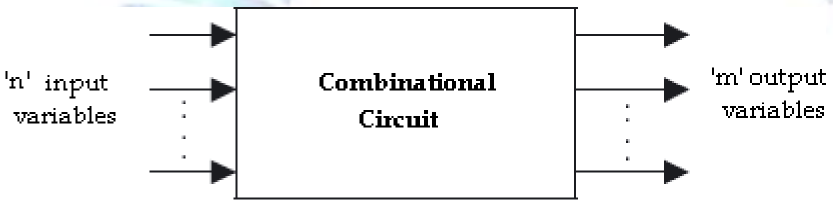
**Combinational circuit** consists of logic gates whose output at any time is determined from the present combination of inputs. The logic gate is the most basic building block of combinational logic. The logical function performed by a combinational circuit is fully defined by a set of Boolean expressions.

**Sequential logic circuit** comprises both logic gates and the state of storage elements such as flip-flops. As a consequence, the output of a sequential circuit depends not only on present value of inputs but also on the past state of inputs.

A combinational circuit consists of input variables, logic gates, and output variables. The logic gates accept signals from inputs and output signals are generated according to the logic circuits employed in it. Binary information from the given data transforms to desired output data in this process. Both input and output are obviously the binary signals, *i.e.*, both the input and output signals are of two possible states, logic 1 and logic 0.

.

**Block diagram of a combinational logic circuit**



For $n$ number of input variables to a combinational circuit, $2^n$ possible combinations of binary input states are possible. For each possible combination, there is one and only one possible output combination. A combinational logic circuit can be described by $m$ Boolean functions and each output can be expressed in terms of $n$ input variables.

# KARNAUGH MAP

## Karnaugh Map(K-Map) method

The **K-map** is a systematic way of simplifying Boolean expressions. With the help of the K-map method, we can find the simplest POS and SOP expression, which is known as the minimum expression. The K-map provides a cookbook for simplification.

Just like the truth table, a K-map contains all the possible values of input variables and their corresponding output values. However, in K-map, the values are stored in cells of the array. In each cell, a binary value of each input variable is stored.

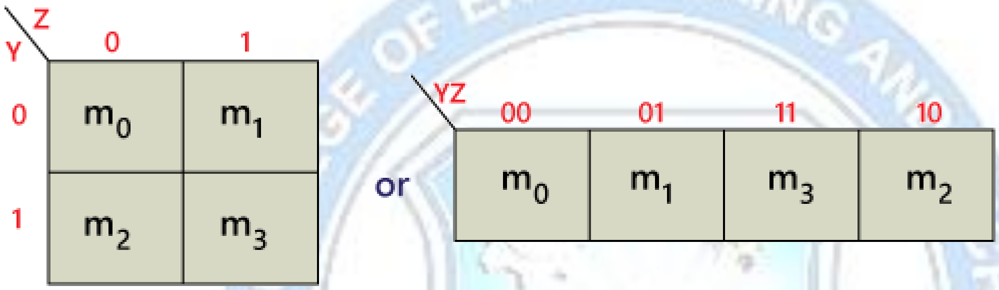
The K-map method is used for expressions containing 2, 3, 4, and 5 variables. For a higher number of variables, there is another method used for simplification called the Quine-McClusky method. In K-map, the number of cells is similar to the total number of variable input combinations. For example, if the number of variables is three, the number of cells is $2^3$=8, and if the number of variables is four, the number of cells is $2^4$. The K-map takes the SOP and POS forms. The K-map grid is filled using 0's and 1's. The K-map is solved by making groups. There are the following steps used to solve the expressions using K-map:

1. First, we find the K-map as per the number of variables.
2. Find the maxterm and minterm in the given expression.
3. Fill cells of K-map for SOP with 1 respective to the minterms.
4. Fill cells of the block for POS with 0 respective to the maxterm.
5. Next, we create rectangular groups that contain total terms in the power of two like 2, 4, 8, ... and try to cover as many elements as we can in one group.

6. With the help of these groups, we find the product terms and sum them up for the SOP form.

### 2 Variable K-map

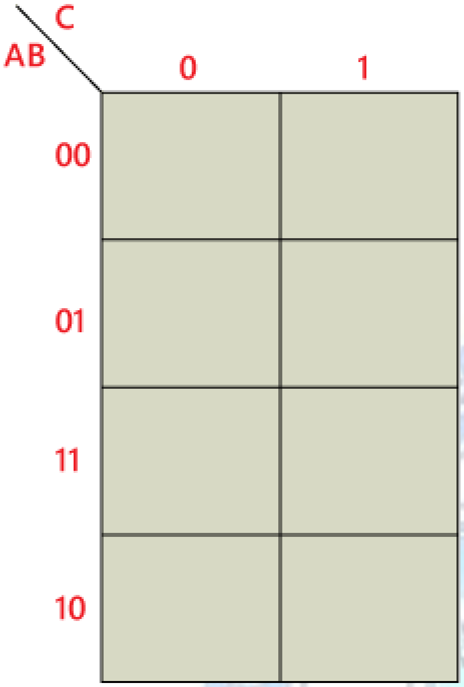
There is a total of 4 variables in a 2-variable K-map. There are two variables in the 2-variable K-map. The following figure shows the structure of the 2-variable K-map:

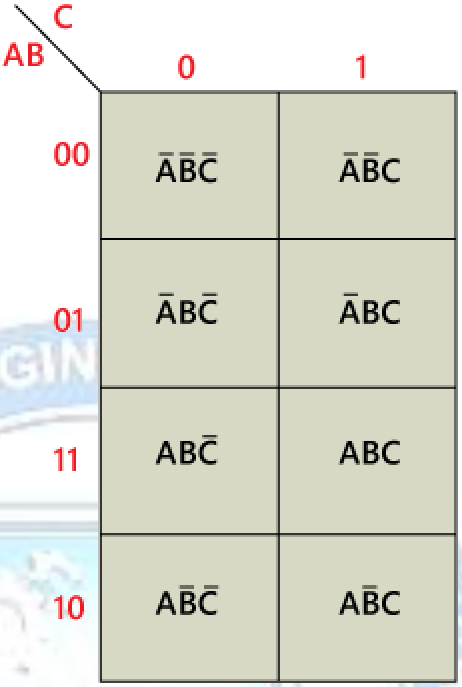


- In the above figure, there is only one possibility of grouping four adjacent minterms.
- The possible combinations of grouping 2 adjacent minterms are {($m_0$, $m_1$), ($m_2$, $m_3$), ($m_0$, $m_2$) and ($m_1$, $m_3$)}.

### 3-variable K-map

The 3-variable K-map is represented as an array of eight cells. In this case, we used A, B, and C for the variable. We can use any letter for the names of the variables. The binary values of variables A and B are along the left side, and the values of C are across the top. The value of the given cell is the binary values of A and B at left side in the same row combined with the value of C at the top in the same column. For example, the cell in the upper left corner has a binary value of 000, and the cell in the lower right corner has a binary value of 101.

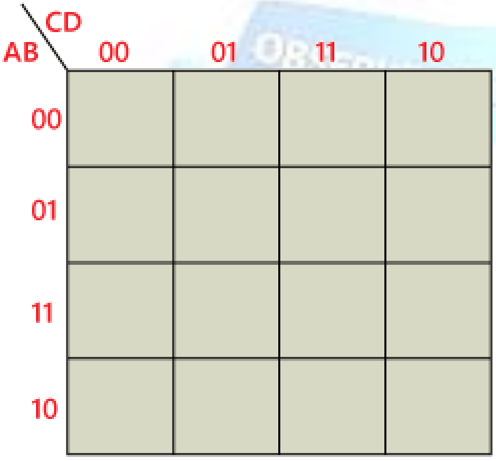


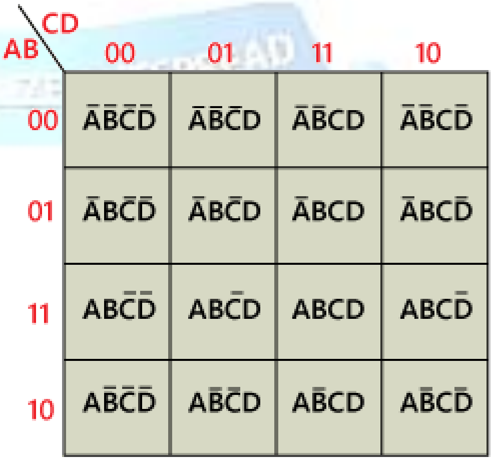


| AB \ C | 0 | 1 |
|---|---|---|
| 00 | $\bar{A}\bar{B}\bar{C}$ | $\bar{A}\bar{B}C$ |
| 01 | $\bar{A}B\bar{C}$ | $\bar{A}BC$ |
| 11 | $AB\bar{C}$ | $ABC$ |
| 10 | $A\bar{B}\bar{C}$ | $A\bar{B}C$ |

## The 4-Variable Karnaugh Map

The 4-variable K-map is represented as an array of 16 cells. Binary values of A and B are along the left side, and the values of C and D are across the top. The value of the given cell is the binary values of A and B at left side in the same row combined with the binary values of C and D at the top in the same column. For example, the cell in the upper right corner has a binary value of 0010, and the cell in the lower right corner has a binary value of 1010





| AB \ CD | 00 | 01 | 11 | 10 |
|---|---|---|---|---|
| 00 | $\bar{A}\bar{B}\bar{C}\bar{D}$ | $\bar{A}\bar{B}\bar{C}D$ | $\bar{A}\bar{B}CD$ | $\bar{A}\bar{B}C\bar{D}$ |
| 01 | $\bar{A}B\bar{C}\bar{D}$ | $\bar{A}B\bar{C}D$ | $\bar{A}BCD$ | $\bar{A}BC\bar{D}$ |
| 11 | $AB\bar{C}\bar{D}$ | $AB\bar{C}D$ | $ABCD$ | $ABC\bar{D}$ |
| 10 | $A\bar{B}\bar{C}\bar{D}$ | $A\bar{B}\bar{C}D$ | $A\bar{B}CD$ | $A\bar{B}C\bar{D}$ |

# ANALYSIS AND DESIGN PROCEDURE

## ANALYSIS PROCEDURE:

Analysis of a combinational circuit determines its functionality which is the logic function that the circuit implements which includes logic diagram, set of Boolean functions, a truth table and an explanation about the circuit operation.

## DESIGN PROCEDURES:

Any combinational circuit can be designed by the following steps of design procedure.

1. The problem is stated.
2. Identify the input and output variables.
3. The input and output variables are assigned letter symbols.
4. Construction of a truth table to meet input -output requirements.
5. Writing Boolean expressions for various output variables in terms of input variables.
6. The simplified Boolean expression is obtained by any method of minimization—algebraic method, Karnaugh map method, or tabulation method.
7. A logic diagram is realized from the simplified Boolean expression using logic gates.

A practical design method has to consider the following constraints:

1. Minimum number of gates
2. Minimum number of inputs to a gate
3. Minimum propagation time of the signal through the circuit.
4. Minimum number of interconnections
5. Limitations of the driving capabilities of each gate.