Pass-Transistor Logic

The implementation of the AND function constructed that way, using only NMOS transistors is shown in Figure 6.33. In this gate, if the B input is high, the top transistor is turned on and copies the input A to the output F. When B is low, the bottom pass transistor is turned on and passes a 0. The switch driven by B seems to be redundant at first glance. Its presence is essential to ensure that the gate is static; this is that a low-impedance path exists to the supply rails under all circumstances, or, in this particular case, when B is low.

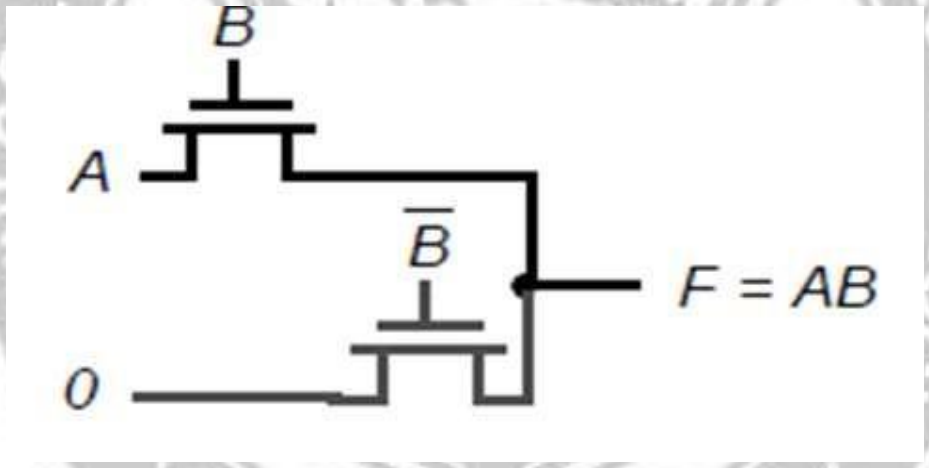

Figure 2.3.1: Pass Transistor

[Source: . R.Jacob Baker, Harry W.LI., David E.Boyee, ―CMOS Circuit Design, Layout and Simulation..]

Differential Pass Transistor Logic

For high performance design, a differential pass-transistor logic family, called CPL or DPL, is commonly used. The basic idea (similar to DCVSL) is to accept true and complementary inputs and produce true and complementary outputs. These gates possess a number of interesting properties:

- XOR's and adders can be realized efficiently with small

number of transistors.

- CPL belongs to the class of static gates
- Modular design
- All gates use same topology

Advantages

- Conceptually simple
- Modular logic style
- Applicability depends on logic function
- Easy to realize adders and multipliers

Disadvantages

- Has routing overhead
- Suffers static power dissipation
- Reduced noise margin

Efficient Pass-Transistor Design

Differential pass-transistor logic, like single-ended pass-transistor logic, suffers from static power dissipation and reduced noise margins, since the high input to the signal-restoring inverter only charges up to VDD-VTn. There are several solutions proposed to deal with this problem as outlined below.

Solution 1: Level Restoration: A common solution to the voltage drop problem is the use of a level restorer, which is a single PMOS configured in a feedback path (Figure 6.39). The gate of the PMOS

device is connected to the output of the inverter, its drain connected to the input of the inverter and

the source to VDD. Assume that node X is at 0V (out is at VDD and the Mr is turned off) with B = VDD and A = 0. If input A makes a 0 to VDD transition, Mn only charges up node X to VDD-VTn. This is, however, enough to switch the output of the inverter low, turning on the feedback device Mr and pulling node X all the way to VDD. This eliminates any static power dissipation in the inverter. Furthermore, no static current path can exist through the level restorer and the pass-transistor, since the restorer is only active when A is high. In summary, this circuit has the advantage that all voltage levels are either at GND or VDD, and no static power is consumed.

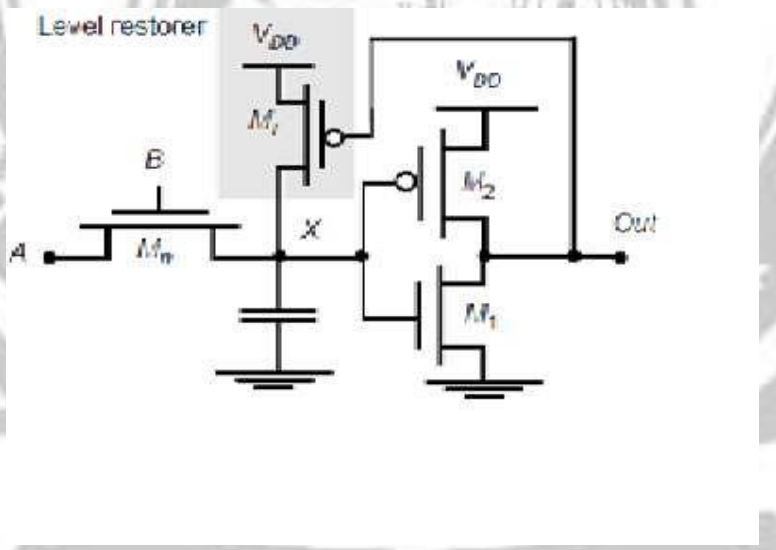

Figure 2.3.2: Level Restoring Circuit

[Source: . R.Jacob Baker, Harry W.LI., David E.Boyee, ―CMOS Circuit Design, Layout and Simulation..]

Solution 2: Multiple-Threshold Transistors: A technology solution to the voltage-drop problem associated with pass-transistor logic is the use of multiple-threshold devices. Using zero threshold devices for

the NMOS pass-transistors eliminates most of the threshold drop, and passes a signal close to VDD. Notice that even if the devices threshold was implanted to be exactly equal to zero, the body effect of the device prevents a swing to VDD. All devices other than the pass transistors (i.e., the inverters) are implemented using standard high-threshold devices.

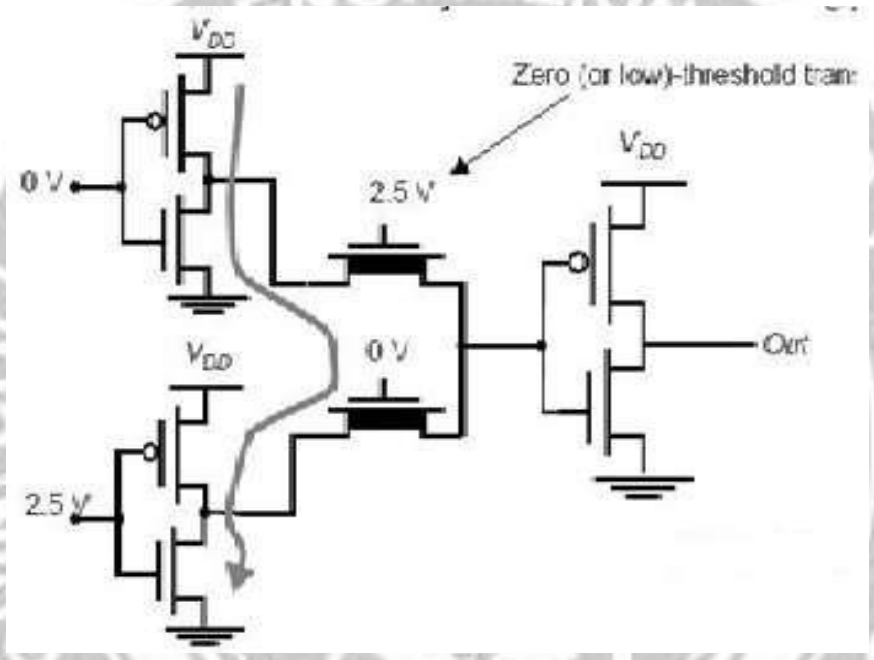

Figure 2.3.3: Static Power Consumption

[Source: . R.Jacob Baker, Harry W.LI., David E.Boyee, ―CMOS Circuit Design, Layout and Simulation..]

Solution 3: Transmission Gate Logic: The most widely-used solution to deal with the voltage- drop problem is the use of transmission gates. It builds on the complementary properties of NMOS and PMOS transistors: NMOS devices pass a strong 0 but a weak 1, while PMOS transistors pass a strong 1 but a weak 0. The ideal approach is to use an NMOS to pull-down and a PMOS to pull-up. This gate either selects

$$\overline{F} = (A \cdot S + B \cdot \overline{S})$$

input A or B based on the value of the control signal S, which is equivalent to

implementing the following Boolean function:

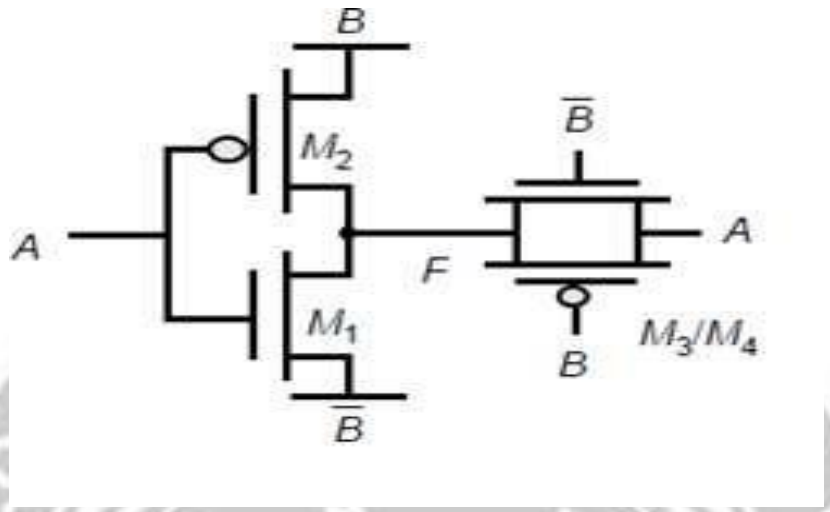

Figure 2.3.4: Transmission Gate XOR

[Source: . R.Jacob Baker, Harry W.LI., David E.Boyee, ―CMOS Circuit Design, Layout and Simulation..]

A complementary implementation of the gate requires eight transistors instead of six.