

## Memory Architecture

### Memory Classification:

Read-Write Memory		Non-Volatile Read-Write Memory	Read-Only Memory
Random Access	Non-Random Access	EEPROM EPROM	Mask-Programmed Programmable (PROM)
SRAM DRAM	FIFO LIFO Shift Register CAN	FLASH	

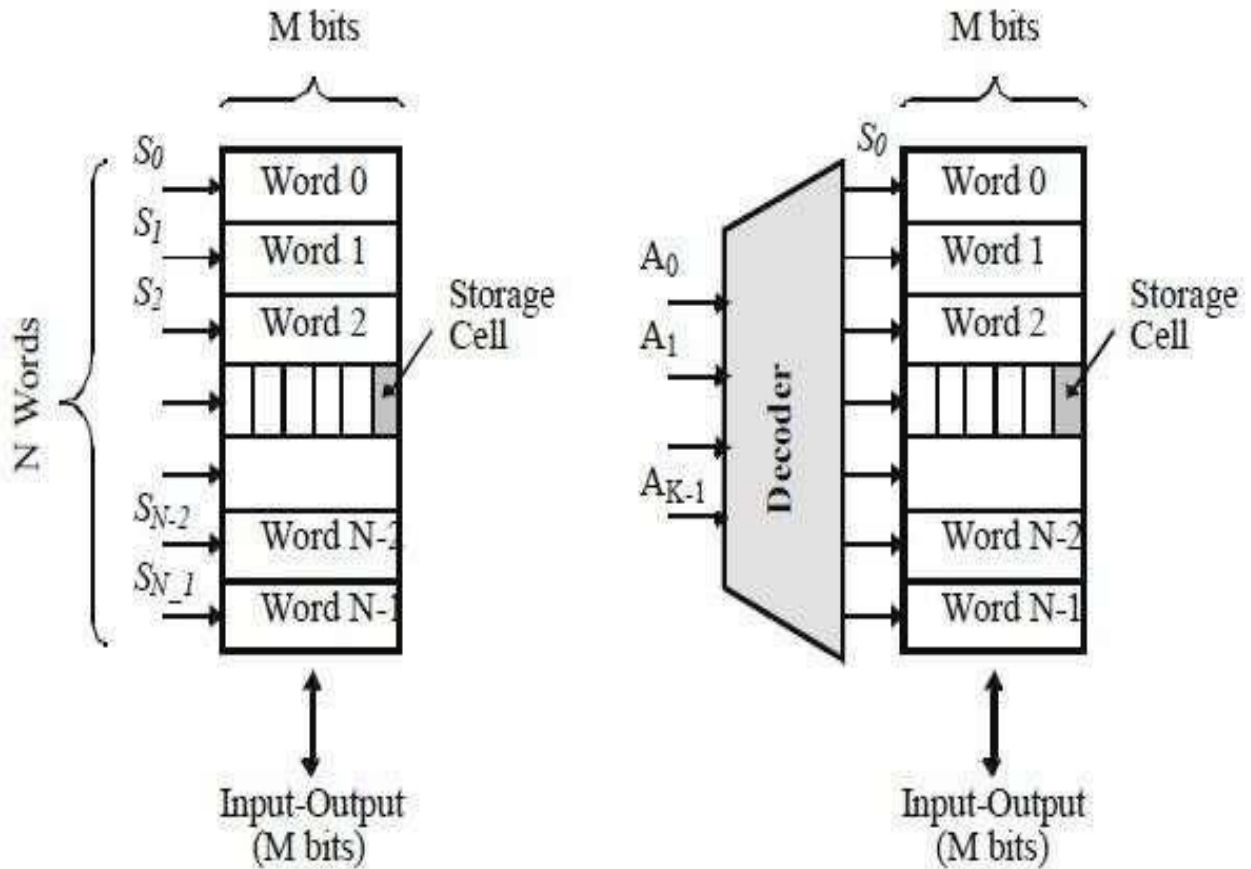
### STATIC (SRAM):

- Data stored as long as supply is applied
- Large (6 transistors/cell)
- Fast
- Differential

### DYNAMIC (DRAM):

- Periodic refresh required
- Small (1-3 transistors/cell)
- Slower
- Single Ended

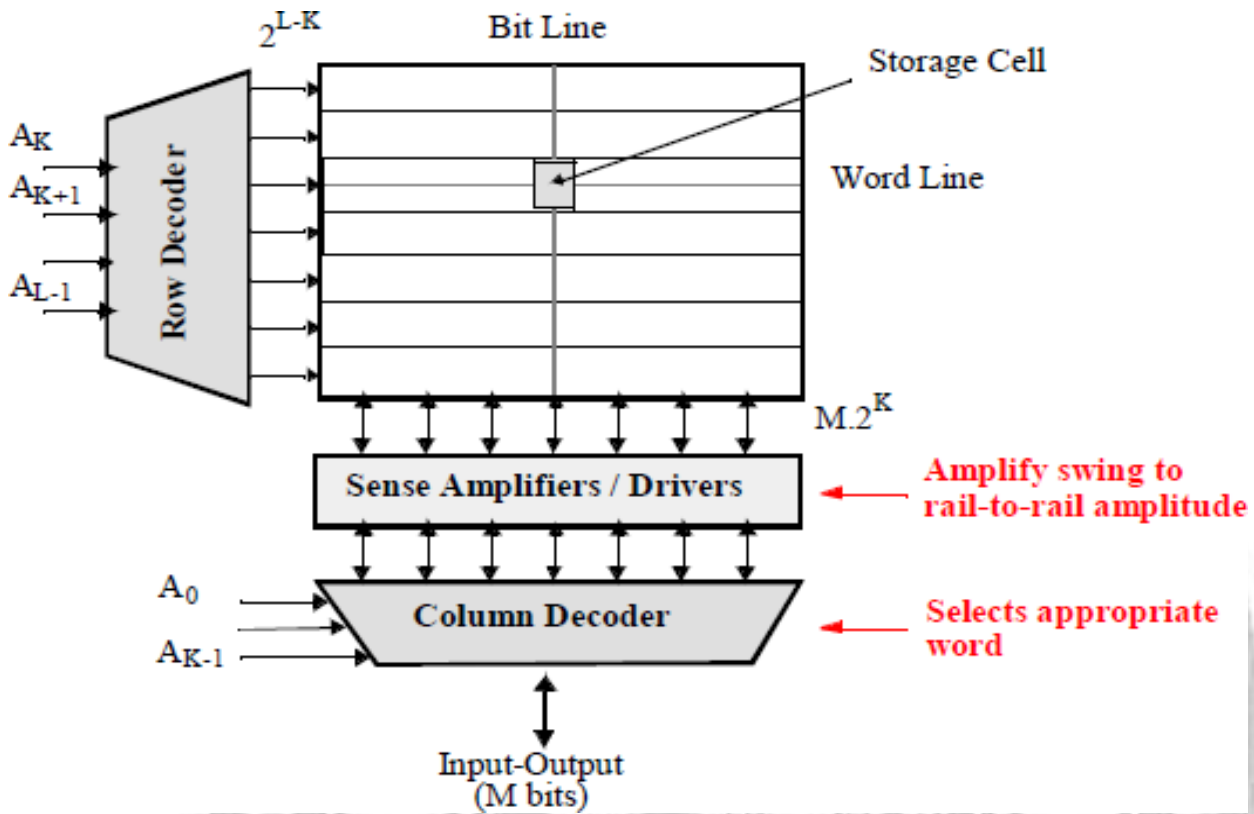
**Memory Architecture: Decoders:**



**N words => N select signals**  
**Too many select signals**

**Decoder reduces # of select signals**  
 $K = \log_2 N$

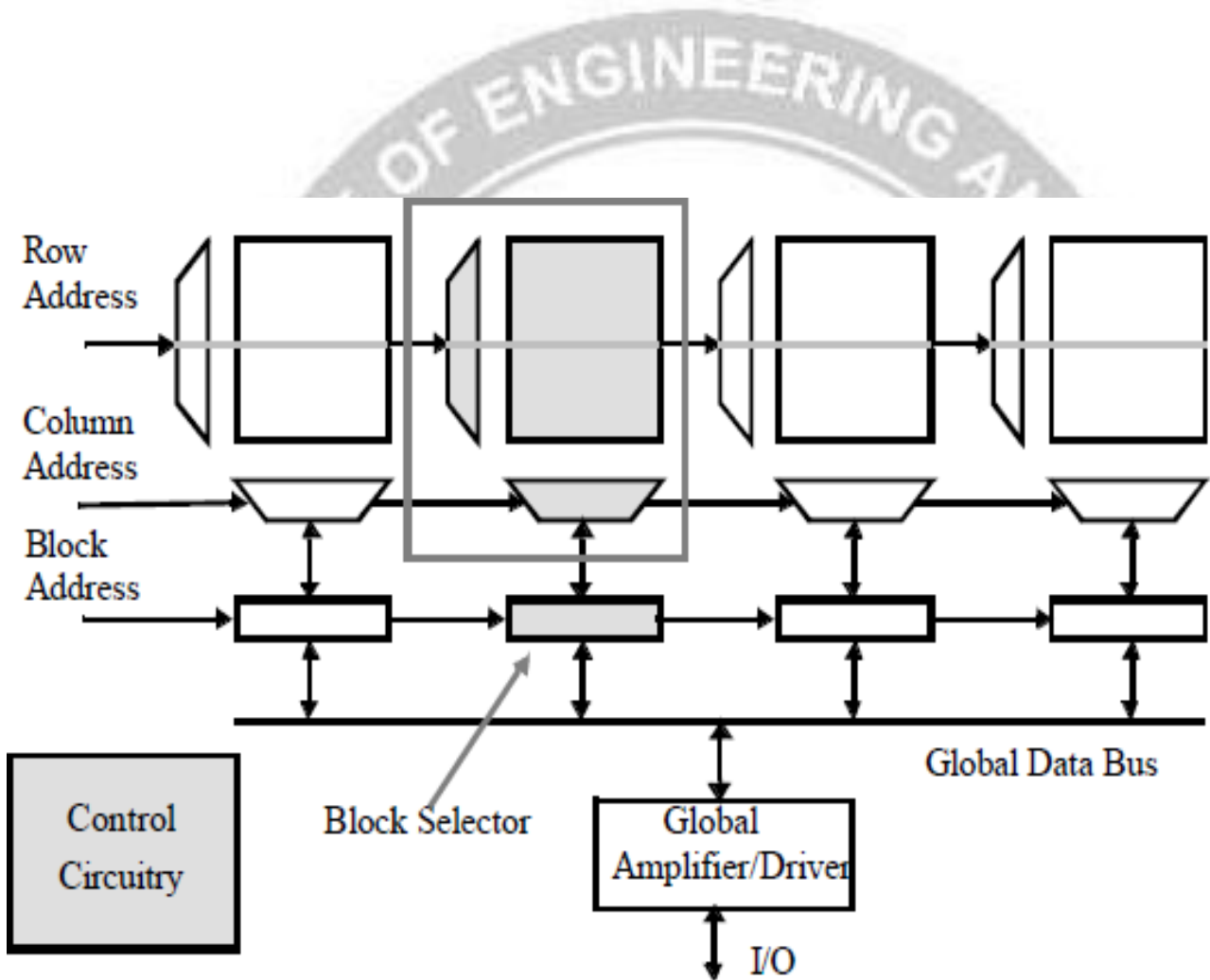




**Fig 4.7.1: Array-Structured Memory Architecture:**

[Source: Sung-Mo kang, Yusuf leblebici, Chulwoo Kim —CMOS Digital Integrated Circuits: Analysis & Design]





**Fig 4.7.2: Hierarchical Memory Architecture**

[Source: Sung-Mo kang, Yusuf leblebici, Chulwoo Kim —CMOS Digital Integrated Circuits:Analysis & Design]

### Advantages:

- Shorter wires within blocks
- Block address activates only one block hence, power savings.

### Tradeoffs

- 1) Speed, area and power can be trade off through the choice of the supply voltages, transistor threshold and device sizes.
- 2) Some design techniques are implemented at design time.
- 3) Transistor widths and lengths can be fixed at the time of design.
- 4) A reduction in supply voltage results in power savings and thus is the most attractive approach.
- 5) Reduced supply evenly lowers the power dissipation of all the logic gates.
- 6) In this approach, non-critical path having timing slack is supplied with low voltage without affecting the system performance.
- 7) Important design concepts: -
  - a) To select right structure before starting an circuit optimization.
  - b) Determine the critical timing path through the circuit.
  - c) Circuit size is not only determined by the number and size of the transistors.
  - d) An obscure optimization can sometimes help to get a better result.
  - e) Power and speed can be traded off through a choice of circuit sizing, supply voltages and transistor threshold