CLASSIFICATION OF ASICS

ASIC - Application Specific Integrated Circuit

- It is an Integrated Circuit (IC) designed to perform a specific function for a specific application.

The ASICs are classified as follows:

I. Full-Custom ASICs

II. Semi-custom ASICs

a. Standard-Cell–Based ASICs (CBIC)

b. Gate-Array–Based ASICs (MPGA)

i. Channelled Gate Array

ii. Channel less Gate Array

iii. Structured Gate Array

III. Programmable ASICs

a. Complex Programmable Logic Devices (CPLD)

b. Field-Programmable Gate Arrays (FPGA)

Full Custom ASIC

- The engineer can design full logic cells in IC.
- So, this technique is known as Full custom ASIC technique.
- Mixed analog and digital technique is used to manufacture IC.
- All the logic cells are specifically designed for one ASIC.
- CMOS is widely used technology to manufacture IC.
- Mixing of analog and digital function are integrated in the same IC for which CMOS technology suits well.
- Designers give importance to performance.
- When large volume is manufactured, overall cost will be reduced.
- In super computer, quality is important so this design is implemented.
- All mask layers are customized in a full-custom ASIC. i.e. for a specific application.
- Generally, the designer lays out all cells by hand
- Some automatic placement and routing may be done
- Critical (timing) paths are usually laid out completely by hand
- Full-custom design offers the *highest performance and lowest part cost* (smallest die size) for a given design.

- The *disadvantages* of full-custom design include *increased design time, complexity, design expense*, and *highest risk.*
- Microprocessors were exclusively full-custom, but designers are increasingly turning to semicustom ASIC techniques in this area as well.

Semi-custom ASICs – Design

- Here all logic cells are predesigned and some of the mask layers are customized.

I. Standard cell based design:

- Standard cells are referred to AND gate, OR gate, multiplexer, flip flop, NOR gate etc.
- Standard cells can be used with larger predefined cells.
- A design is generated automatically from HDL language.
- Then layout is created. In standard cell design, cells are placed in rows, and rows are separated by routing channel.
- All cells in library are in identical heights, widths of the cells can be varied to accommodate for variations in complexity between cells.
- A substantial fraction of area is allotted for signal routing.

II. Gate Array Based ASICs:

Gate array is known as GA.

- In GA based ASIC, the transistors are predefined on the silicon wafer.
- Base array: the predefined pattern of transistors on a gate is known as base array.
- Base cell: the small element which is replicated to make the base array is known as base cell or primitive cell.
- Masked Gate array: Interconnect is defined by using top few layers of metal. This type of gate array is known as masked gate array.
- Gate array library is provided by ASIC Company.
- The designer can choose the predefined logic cells from a gate array library. These logic cells are known as Macros.
- Cell-layout is same for each logic cell. But interconnect is customized.
- It is also called as pre-diffused array because the transistors are diffused at first.

Types of MPGAs (Mask Programmable Gate Arrays):

Channeled Gate Array

Channel less Gate Array

Structured Gate Array

Channeled Gate Array:

- It is similar to CBIC (cell based ASIC).

- The rows of cells are separated by channels.
- These channels are used for interconnect.
- Space between rows of cells is fixed in a channeled gate array.
- But space between rows of cells may be adjusted in a CBIC.

Features:

- Only interconnect is customized.
- The interconnect uses predefined spaces between rows of base cells.
- Manufacturing lead time is between two days and two weeks.

Channel less Gate Array:

- Channel less Gate Array is also called as channel free GA.
- In this array, there is no predefined space between rows for routing.
- Top few layers are used for defining interconnect connections.
- There are no predefined areas set aside for routing - routing is over the top of the gate-array devices.
- Each logic cell or macro in a gate-array library is predesigned using fixed tiles of transistors known as the gate-array base cell (or just base cell).
- Channeled and channel less gate arrays may use either gate isolation or oxide isolation.
- Isolate the transistors on a gate array from one another either with thick field oxide or by using other transistors that are wired permanently off.

Structured Gate Array:

- Structured Gate Array is also called as embedded gate array or master slice or master image gate.
- It combines some of the features of CBIC and Masked gate array (MGA).
- In this array, some of the area is used for implementation of specially designed embedded block.
- Embedded area either can contain a different base cell that is more suitable for building memory cells, or a complete circuit block, such as a microcontroller.

Special features:

- Only the interconnect is customized
- Custom block can be embedded
- Manufacturing lead time is 2 days to 2 weeks
- Area efficiency is increased
- Performance is increased with low cost

Disadvantages:

- The embedded function is fixed.
- For ex: if embedded block has 32K bit memory. But the customer needs only 18K bit, the 16K memory is wasted.