CLASSIFICATIONOFSYNCHRONOUSSEQUENTIALCIRCUIT:

In synchronous or clocked sequential circuits, clocked Flip-Flops are used as memory elements, which change their individual states in synchronism with the periodic clock signal. Therefore, the change in states of Flip-Flop and change in state of the entire circuits accurate the transition of the clock signal.

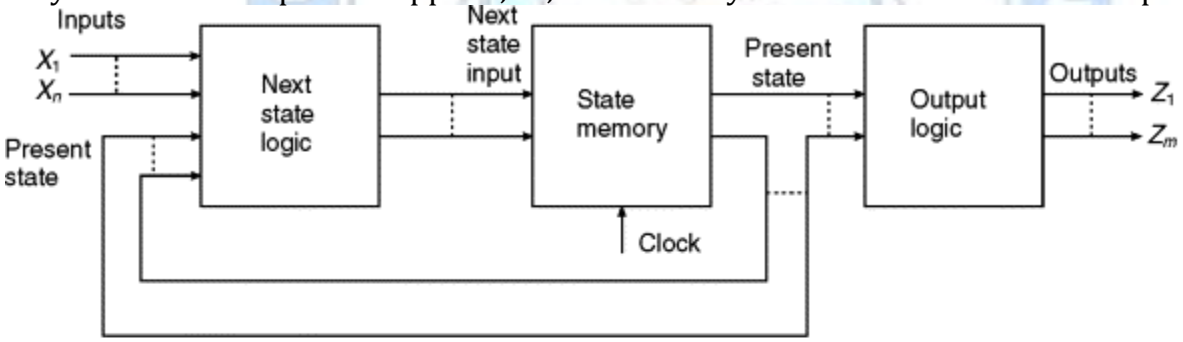
The synchronous or clocked sequential networks are represented by two models.

Moore model: The output depends only on the present state of the Flip-Flops.

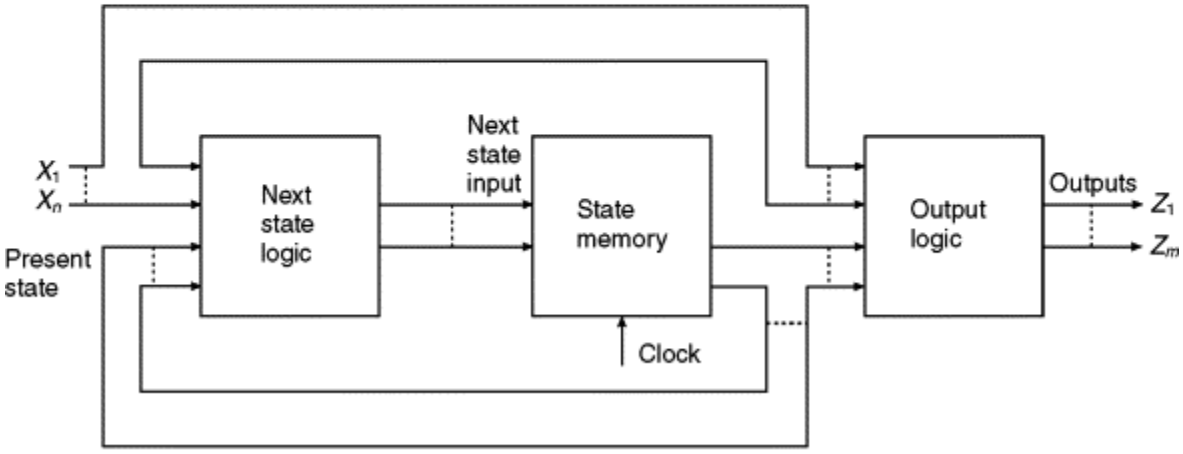
Mealy model: The output depends on both the present state of the Flip-Flops and on the inputs

Moore model:

In the Moore model,the outputs are a function of the present state of the Flip-Flops only.The out put depends only on present state of FlipFlops,it a ppears onlyafter the clock pulse is applied,i.e.,it varies in synchronism with the clock input.



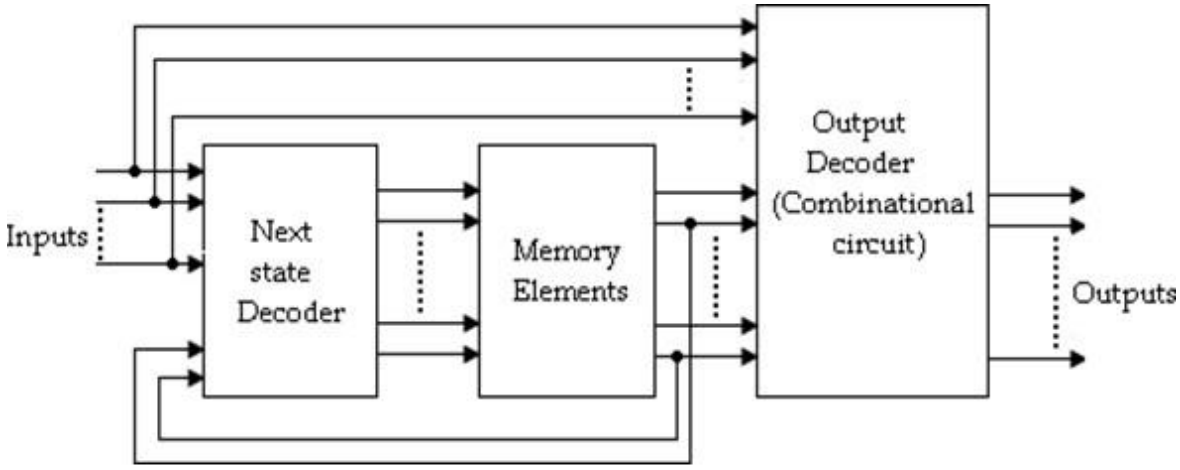
(a)



(b)

Mealymodel:

In the Mealymodel , the outputs are functions of both the present state of the Flip-Flops and inputs



Mealy model

Difference between Moore and Mealymodel

S.No	Moore model	Mealy model
1	Its output is a function of present State only.	Its output is a function of present state As well as present input.
2	An input change does not affect the output.	Input changes may affect the output of The circuit.
3	It requires more number of states For implementing same function.	It requires less number of states for Implementing same function.

ANALYSIS OF SYNCHRONOUS SEQUENTIAL CIRCUIT:

ANALYSIS PROCEDURE:

The synchronous sequential circuit analysis is summarizes as given below:

1. AssignastatevariabletoeachFlip-Flopinthesynchronoussequentialcircuit.
2. Write the excitation input functions for each Flip-Flop and also write the Moore/Mealy output equations.
3. Substitute the excitation input functions into the b is table equations for the Flip- Flops to obtain the next state output equations.
4. Obtain the state table and reduced form of the state table.

5. Draw the state diagram by using the second form of the state table.

ANALYSISOFMEALYMODEL:

A sequential circuit has two JK Flip-Flops A and B, one input(x) and one output(y).

1. A sequential circuit has two JK Flip-Flops A and B, one input(x) and one output the Flip-Flop input functions are,

$J_A = B + x$ $J_B = A' + x'$

$K_A = 1$ $K_B = 1$

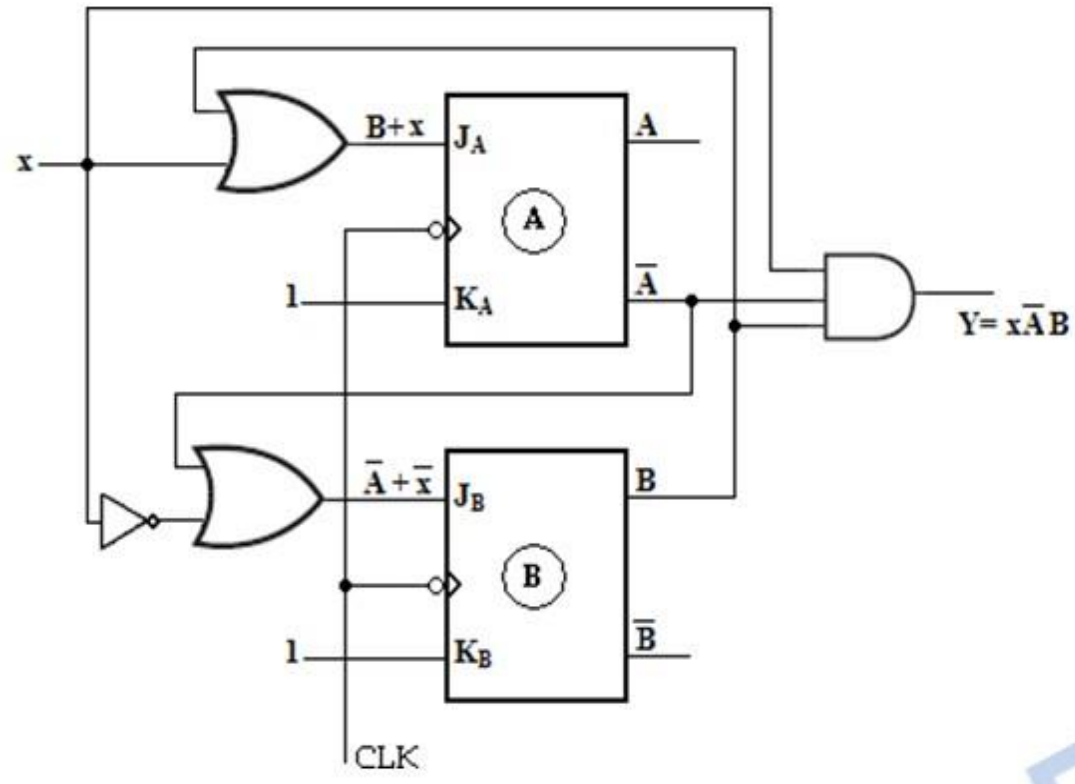
And the circuit output function, $Y = x A'B$.

a) Draw the logic diagram of the Mealy circuit,

b) Tabulate the state table,

c) Draw the state diagram.

Logic Diagram:



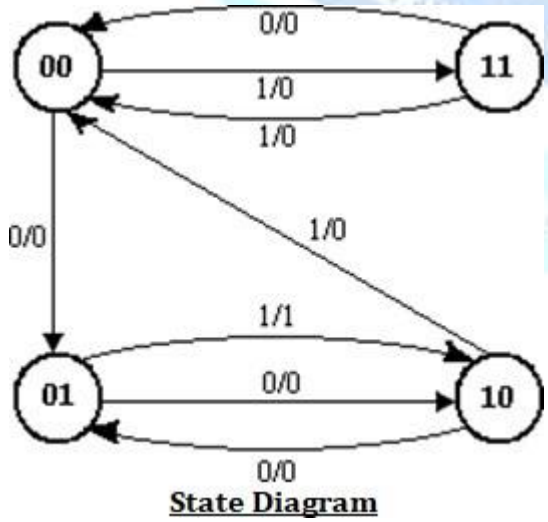
State table:

Present state		Input	Flip-Flop Inputs				Next state		Output
A	B	x	JA=B+x	KA=1	JB=A'+x'	KB=1	A(t+1)	B(t+1)	Y=xA'B
0	0	0	0	1	1	1	0	1	0
0	0	1	1	1	1	1	1	1	0
0	1	0	1	1	1	1	1	0	0
0	1	1	1	1	1	1	1	0	1
1	0	0	0	1	1	1	0	1	0
1	0	1	1	1	0	1	0	0	0
1	1	0	1	1	1	1	0	0	0
1	1	1	1	1	0	1	0	0	0

Reduced State Table

Present state		Next state				Output	
		x=0		x=1		x=0	x=1
A	B	A	B	A	B	y	y
0	0	0	1	1	1	0	0
0	1	1	0	1	0	0	1
1	0	0	1	0	0	0	0
1	1	0	0	0	0	0	0

State Diagram:



State Diagram

2. A sequential circuit with two 'D' Flip-Flops A and B, one input(x) and one

output(y). The Flip-Flop input functions are:

$D_A = Ax + B$

$xD_B = A'x$

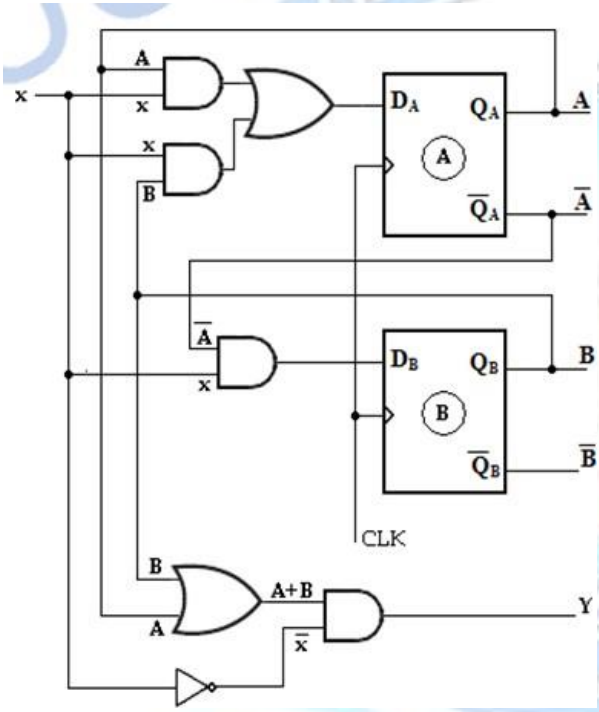
and the circuit output function is, **Y=(A+B)x'**.

(a) Draw the logic diagram m of the circuit,

(b) Tabulate the state table,

(c) Draw the state diagram.

3. Soln:



Present state		Input	Flip-FlopInputs		Nextstate		Output
A	B	x	D_A= Ax+Bx	D_B=A'x	A(t+1)	B(t+1)	Y=(A+B)x'
0	0	0	0	0	0	0	0
0	0	1	0	1	0	1	0
0	1	0	0	0	0	0	1
0	1	1	1	1	1	1	0
1	0	0	0	0	0	0	1
1	0	1	1	0	1	0	0
1	1	0	0	0	0	0	1
1	1	1	1	0	1	0	0

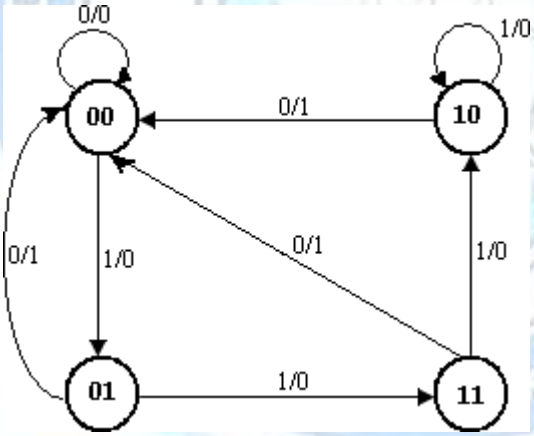
Present state		Nextstate				Output	
		x=0		x=1		x=0	x=1
A	B	A	B	A	B	Y	Y
0	0	0	0	0	1	0	0
0	1	0	0	1	1	1	0
1	0	0	0	1	0	1	0
1	1	0	0	1	0	1	0

Second for m of state table

State Diagram:

Second for m of state table

State Diagram:



3. A sequential circuit has two JK Flip-Flop A and B. the Flip-Flop input functions are: $J_A=B$ $J_B=x'$

$K_A=Bx'$ $K_B=A \oplus x$.

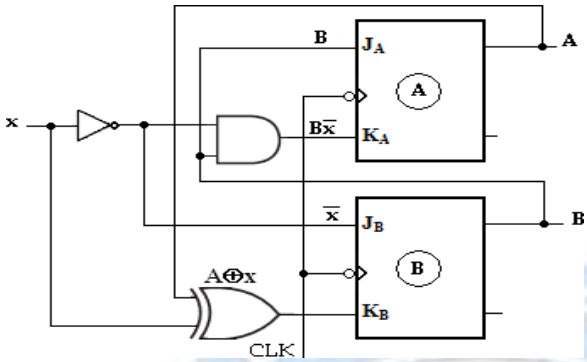
(a) Draw the logic diagram of the circuit,

(b) Tabulate the state table,

(c) Draw the state diagram.

Soln:

Logic diagram



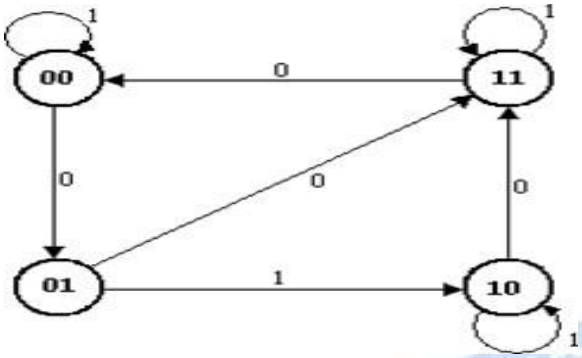
The output function is not given in the problem. The output of the Flip-Flops maybe considered as the output of the circuit.

State table:

Present state		Input	Flip-Flop Inputs				Next state	
A	**B**	**x**	**J_A=B**	**K_A=Bx'**	**J_B= x'**	**K_B=A x**	**A(t+1)**	**B(t+1)**
0	0	0	0	0	1	0	0	1
0	0	1	0	0	0	1	0	0
0	1	0	1	1	1	0	1	1
0	1	1	1	0	0	1	1	0
1	0	0	0	0	1	1	1	1
1	0	1	0	0	0	0	1	0
1	1	0	1	1	1	1	0	0
1	1	1	1	0	0	0	1	1

Present state		Next state			
		X = 0		**X = 1**	
A	**B**	**A**	**B**	**A**	**B**
0	0	0	1	0	0
0	1	1	1	1	0
1	0	1	1	1	0
1	1	0	0	1	1

State Diagram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