# DSP ARCHITECTURE

## Types of Architecture

- There are three types of standard architectures for microprocessors. They are,

### (i) Von-Neumann architecture

- General Purpose Processors normally have these types of architectures. The architecture share same memory for program and data. The processor performs instruction fetch, decode and execute operations sequentially. In such architecture, speed can be increased by pipelining. This type of architecture contains common interval address and data bus, ALU, Accumulator, I/O devices and common memory for program and data. This type of architecture is not suitable for DSP.

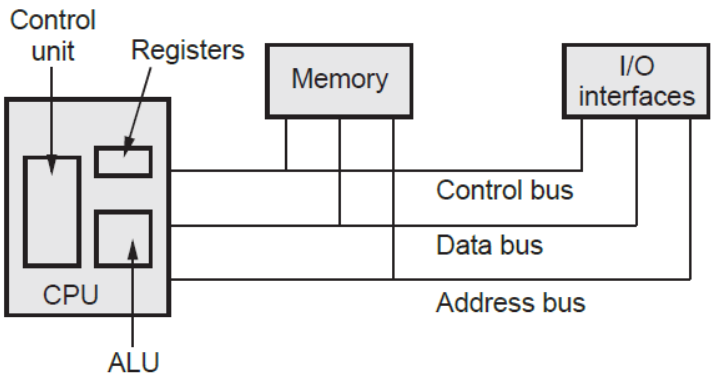


**Fig. Von-Neumann architecture**

### (ii) Harvard architecture

- The Harvard architecture has separate memory for program and data. There are also separate address bus for program and data. Because of these separate on chip memories and internal buses, the speed of execution in Harvard architecture is high.

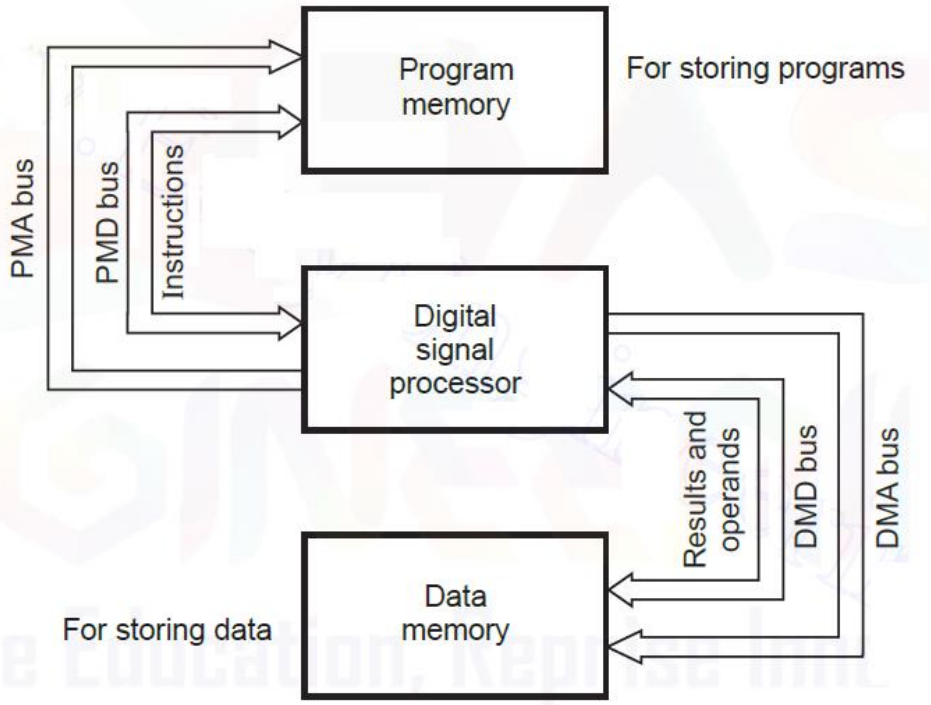


**Fig. Harvard architecture**

- From the Fig. it is observed that there is Program Memory Address (PMA) bus and Program Memory Data (PMD) bus separate for program memory. Similarly there is separate Data Memory Data (DMD) bus and Data Memory Address (DMA) bus for data memory. This is all on chip. The digital signal processor includes various registers, address generators, ALUs etc.
- The Harvard architecture has multiple bus structure and separate memories. Hence its speed is increased. It is possible to fetch next instruction when current instruction is executed. That is, the fetch, decode and execute operations are done in parallel.

**(iii) Modified Harvard architecture**

- In this architecture data memory can be shared by data as well as programs. Fig illustrates this concept.

- Normally the program memory and data memory addresses are generated by separate address generators. The data address generator for programs can address program memory as well as data memory. This provides flexibility in use of these memories. The speed of operation is also increased. The architecture is shown in Fig. 5.3.3 is normally on chip. Today's commonly used DSP processors normally have this type of architecture.

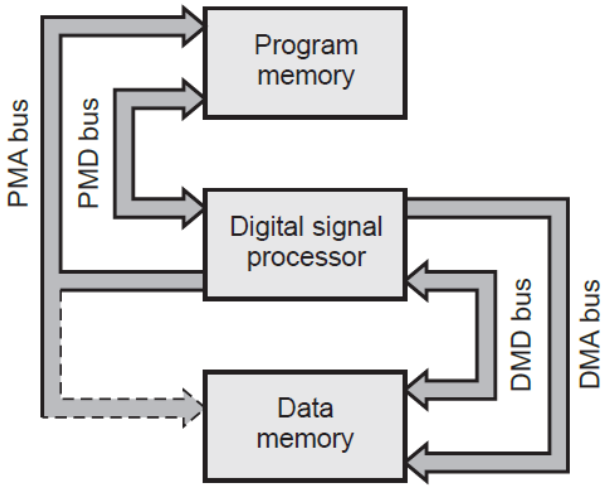


**Fig. Modified Harvard architecture data memory shared by programs**