UNIT III

FIELD EFFECT TRANSISTORS

Field effect devices are those in which current is controlled by the action of an electron field, rather than carrier injection.

Field-effect transistors are so named because a weak electrical signal coming in through one electrode creates an electrical field through the rest of the transistor.

The FET was known as a ‐unipolar‖ transistor because the function depends only on minority carriers.

The term refers to the fact that current is transported by carriers of one polarity (majority), whereas in the conventional bipolar transistor carriers of both polarities (majority and minority) are involved.

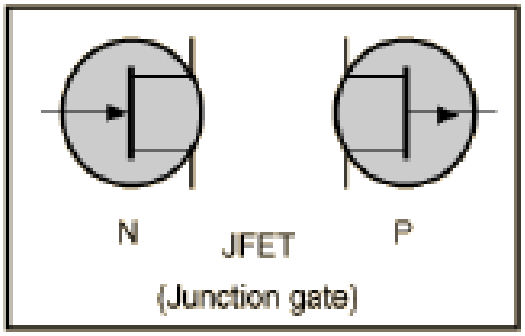
The family of FET devices may be divided into :

• Junction FET

• Depletion Mode MOSFET

Enhancement Mode MOSFET

Junction FETs (JFETs)



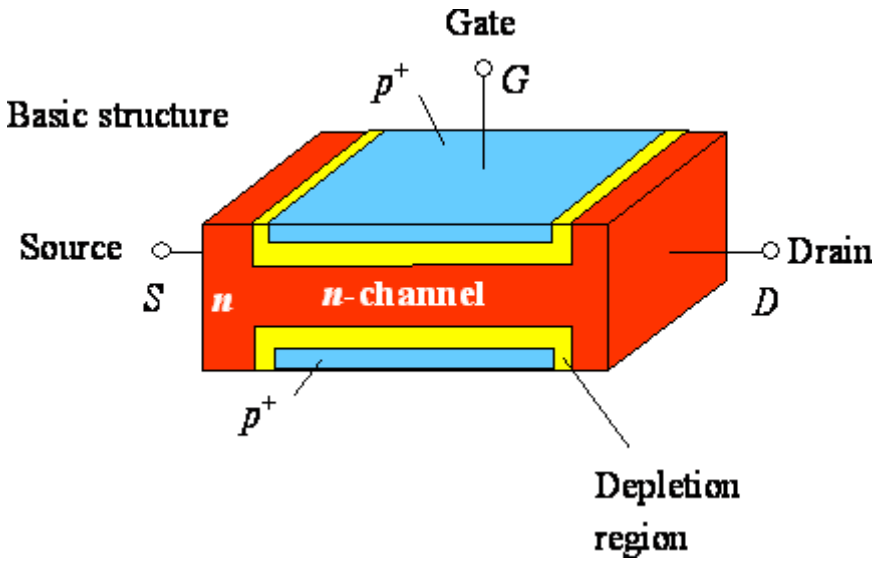
JFETs consists of a piece of high-resistivity semiconductor material (usually Si) which constitutes a channel for the majority carrier flow.

Conducting semiconductor channel between two ohmic contacts – source & drain.

JFET is a high-input resistance device, while the BJT is comparatively low.

If the channel is doped with a donor impurity, n-type material is formed and the channel current will consist of electrons.

If the channel is doped with an acceptor impurity, p-type material will be formed and the channel current will consist of holes.



N-channel devices have greater conductivity than p-channel types, since electrons have higher mobility than do holes; thus n-channel JFETs are approximately twice as efficient conductors compared to their p-channel counterparts.

The magnitude of this current is controlled by a voltage applied to a gate, which is a reverse-biased.

The fundamental difference between JFET and BJT devices: when the JFET junction is reverse-biased the gate current is practically zero, whereas the base current of the BJT is always some value greater than zero.

Basic structure of JFETs

• In addition to the channel, a JFET contains two ohmic contacts: the source and the drain.

• The JFET will conduct current equally well in either direction and the source and drain leads are usually interchangeable. N-channel JFET

• This transistor is made by forming a channel of N-type material in a P-type substrate.

• Three wires are then connected to the device.

• One at each end of the channel.

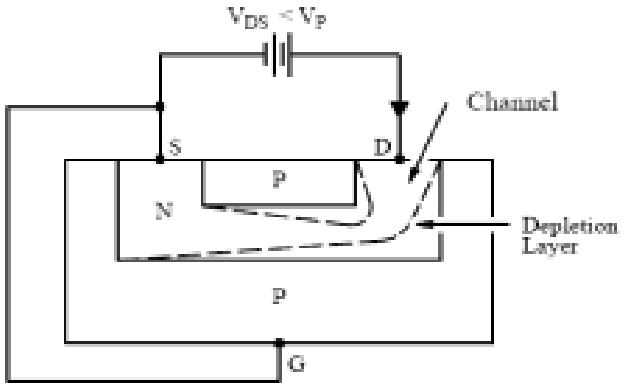
• One connected to the substrate.

In a sense, the device is a bit like a PN-junction diode, except that there are two wires connected to the N-type side

• The gate is connected to the source.

• Since the pn junction is reverse-biased, little current will flow in the gate connection.

• The potential gradient established will form a depletion layer, where almost all the electrons present in the n-type channel will be swept away. The most depleted portion is in the high field between the G and the D, and the least-depleted area is between the G and the S.



• Because the flow of current along the channel from the (+ve) drain to the (-ve) source is really a flow of free electrons from S to D in the n-type Si, the magnitude of this current will fall as more Si becomes depleted of free electrons.

• There is a limit to the drain current (ID) which increased VDS can drive through the channel.

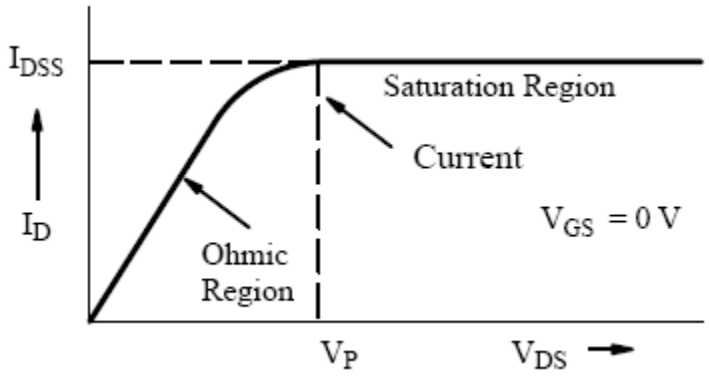
• This limiting current is known as IDSS (*Drain-to-Source current with the gate shorted to the source*).

• The output characteristics of an n-channel JFET with the gate short-circuited to the source.

• The initial rise in ID is related to the buildup of the depletion layer as VDS increases.

• The curve approaches the level of the limiting current IDSS when ID begins to be pinched off.

• The physical meaning of this term leads to one definition of pinch-off voltage, VP , which is the value of VDS at which the maximum IDSS flows.



• With a steady gate-source voltage of 1 V there is always 1 V across the wall of the channel at the source end.

• A drain-source voltage of 1 V means that there will be 2 V across the wall at the drain end. (The drain is ‗up' 1V from the source potential and the gate is 1V ‗down', hence the total difference is 2V.)

• The higher voltage difference at the drain end means that the electron channel is squeezed down a bit more at this end.

• When the drain-source voltage is increased to 10V the voltage across the channel walls at the drain end increases to 11V, but remains just 1V at the source end.

• The field across the walls near the drain end is now a lot larger than at the source end.

• As a result the channel near the drain is squeezed down quite a lot.

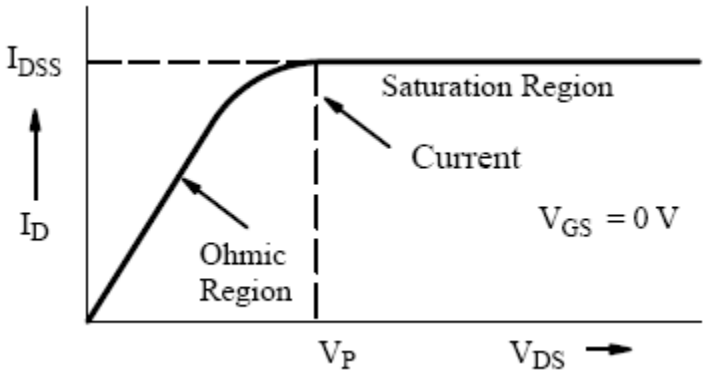
• Increasing the source-drain voltage to 20V squeezes down this end of the channel still more.

• As we increase this voltage we increase the electric field which drives electrons along the open part of the channel.

• However, also squeezes down the channel near the drain end.

• This reduction in the open channel width makes it harder for electrons to pass.

• As a result the drain-source current tends to remain constant when we increase the drain source voltage.



• Increasing VDS increases the widths of depletion layers, which penetrate more into channel and hence result in more channel narrowing toward the drain.

• The resistance of the n-channel, RAB therefore increases with VDS.

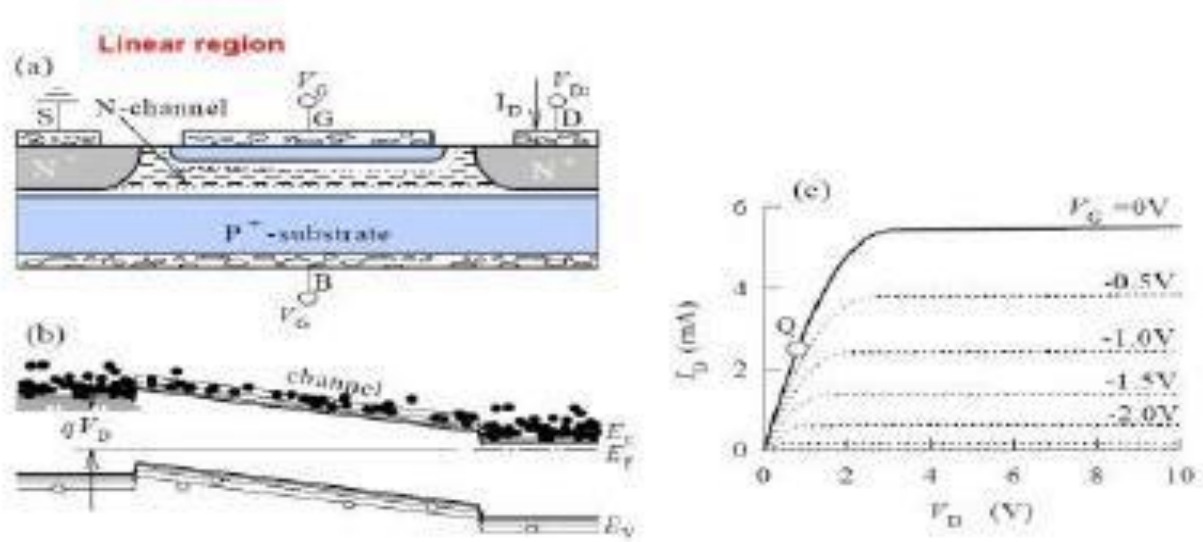
• The drain current: IDS = VDS/RAB

• ID versus VDS exhibits a sub linear behavior, see figure for VDS < 5V.

• The pinch-off voltage, VP is the magnitude of reverse bias needed across the p+n junction to make them just touch at the drain end.

• Since actual bias voltage across p+n junction at drain end is VGD, the pinch-off occur whenever: VGD = -VP.

JFET: I-V characteristics



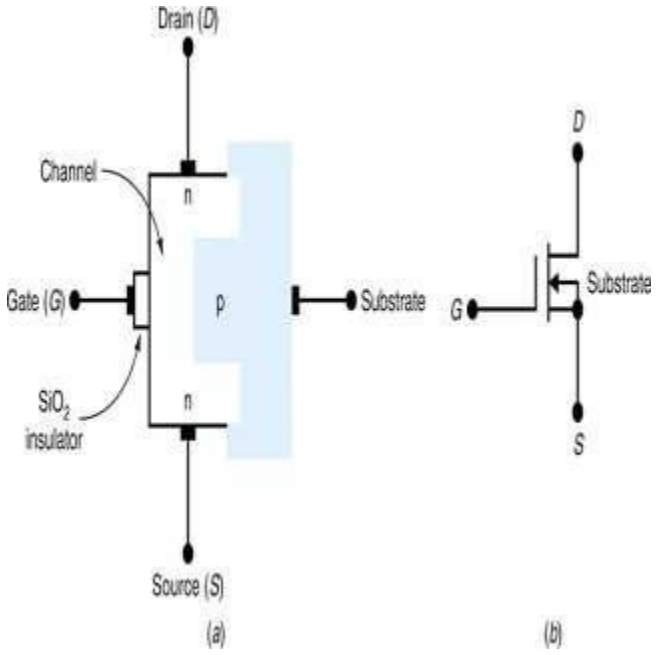
<u>MOSFETs and Their Characteristics</u>

The metal-oxide semiconductor field effect transistor has a gate, source, and drain just like the JFET.

The drain current in a MOSFET is controlled by the gate-source voltage VGS.
There are two basic types of MOSFETS: the enhancement-type and the depletion-type.

The enhancement-type MOSFET is usually referred to as an E-MOSFET, and the depletion type, a D-MOSFET.

The MOSFET is also referred to as an IGFET because the gate is insulated from the channel



DEPLETION-TYPE MOSFET

MOSFETs are further broken down into depletion type and enhancement type. The terms depletion and enhancement define their basic mode of operation, while the label MOSFET stands for metal-oxide-semiconductor-field-effect transistor.

Basic Construction

The basic construction of the n-channel depletion-type MOSFET is provided in Fig. A slab of p-type material is formed from a silicon base and is referred to as the substrate. It is the foundation upon which the device will be constructed. In some cases the substrate is internally

connected to the source terminal. However, many discrete devices provide an additional terminal labeled SS, resulting in a four-terminal device, such as that appearing in Fig. 1

The source and drain terminals are connected through metallic contacts to n-doped regions linked by an n-channel as shown in the figure. The gate is also connected to a metal contact surface but remains insulated from the n-channel by a very thin silicon dioxide (SiO_2) layer.

SiO_2 is a particular type of insulator referred to as a dielectric that sets up opposing (as revealed by the prefix di-) electric fields within the dielectric when exposed to an externally applied field.

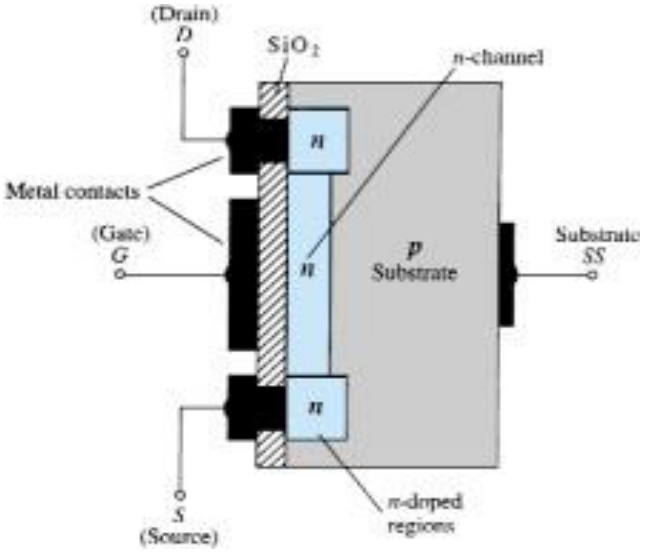


Fig. 1 n – channel depletion type MOSFET

There is no direct electrical connection between the gate terminal and the channel of a MOSFET.

It is the insulating layer of SiO2 in the MOSFET construction that accounts for the very desirable high input impedance of the device.

Basic Operation and Characteristics

In Fig. 2 the gate-to-source voltage is set to zero volts by the direct connection from one terminal to the other, and a voltage VDS is applied across the drain-to-source terminals.

The result is an attraction for the positive potential at the drain by the free electrons of the n-channel and a current similar to that established through the channel of the JFET. In fact, the resulting current with V_{GS} = 0 V continues to be labeled IDSS, as shown in Fig. 3.

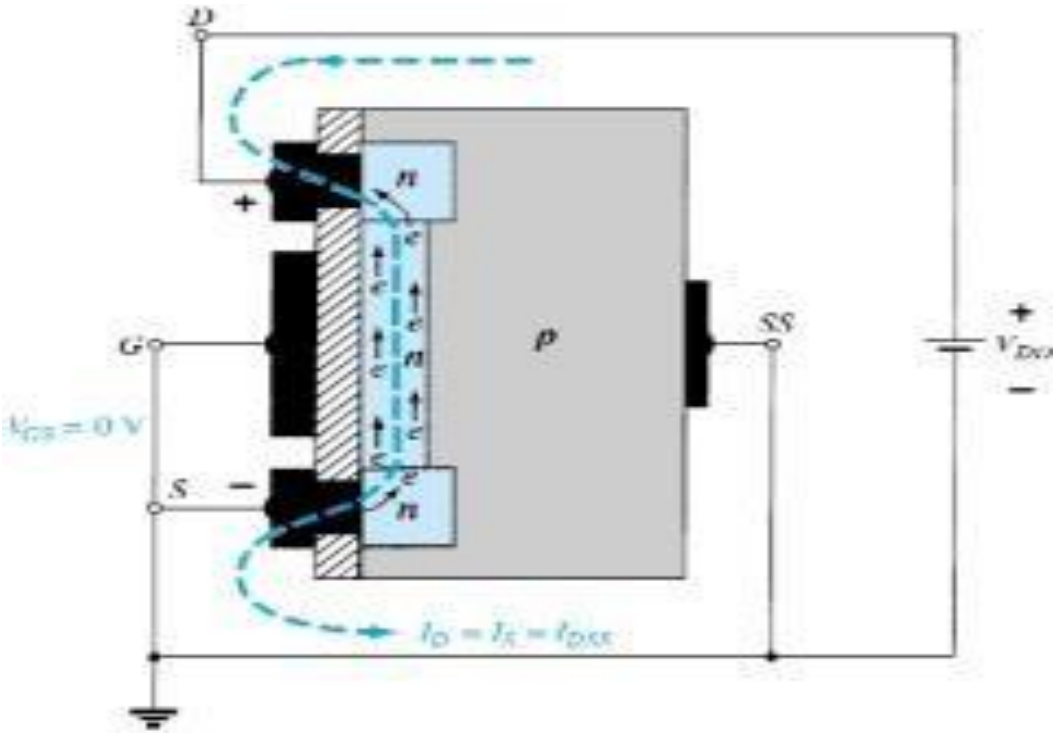


Fig 2. n – channel depletion type MOSFET with $V_{GS} = 0$ V

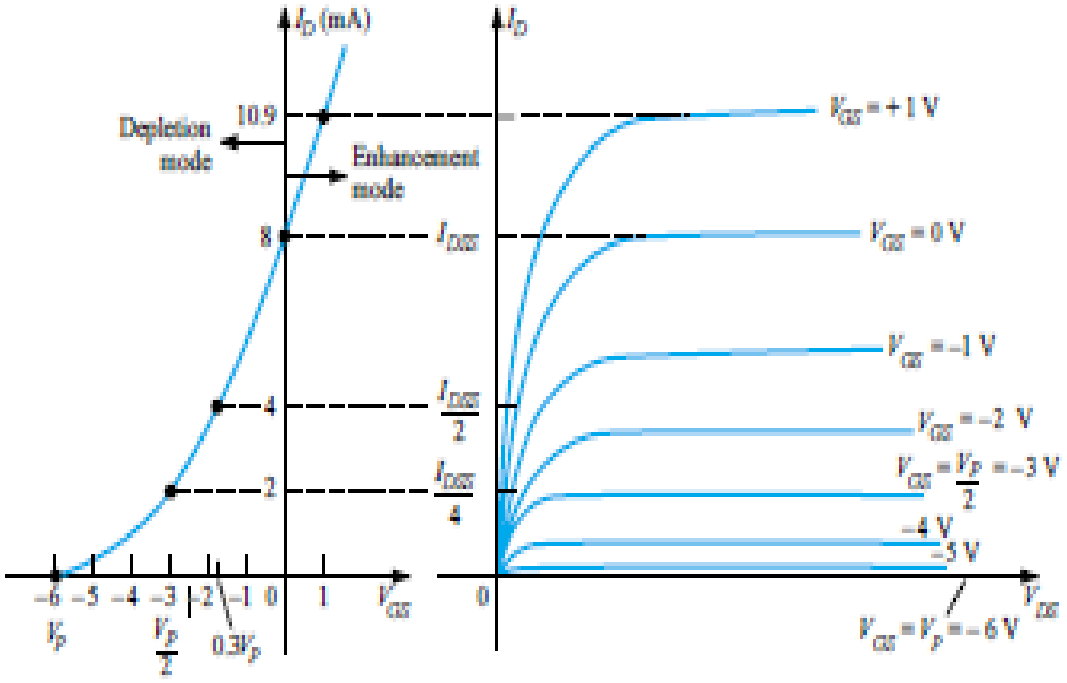


Fig 3. Drain and transfer characteristics

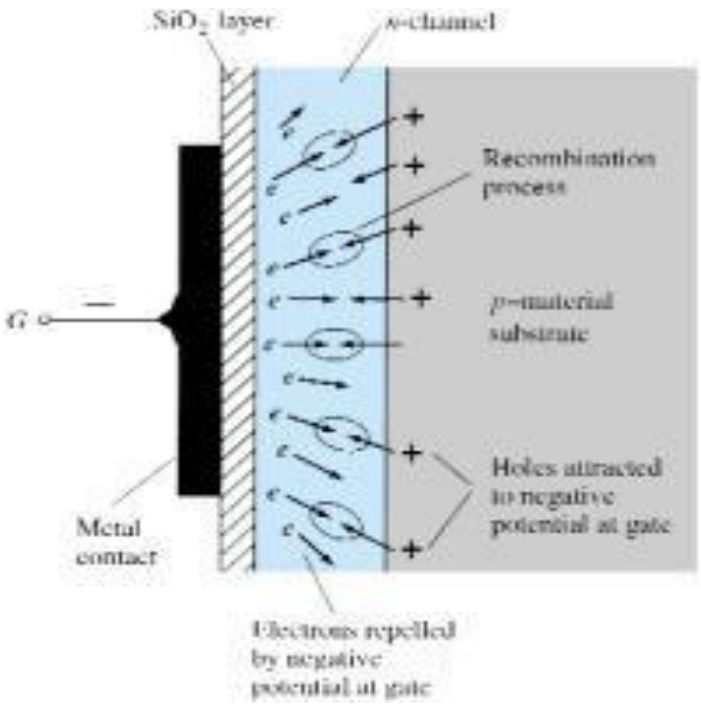


Fig.4 Reduction in free carriers in channel due to –ve potential

In Fig. 4, VGS has been set at a negative voltage such as -1 V. The negative potential at the gate will tend to pressure electrons toward the p-type substrate (like charges repel) and attract holes from the p-type substrate (opposite charges attract) as shown in Fig. 4. Depending on the magnitude of the negative bias established by V_{GS}, a level of recombination between electrons and holes will occur that will reduce the number of free electrons in the n-channel available for conduction. The more negative the bias, the higher the rate of recombination.

For positive values of V_{GS}, the positive gate will draw additional electrons (free carriers) from the p-type substrate due to the reverse leakage current and establish new carriers through the collisions resulting between accelerating particles. As the gate-to-source voltage continues to increase in the positive direction, Fig. 3 reveals that the drain current will increase at a rapid rate.

ENHANCEMENT-TYPE MOSFET

Basic Construction

The basic construction of the n-channel enhancement-type MOSFET is provided in Fig.1. A slab of p-type material is formed from a silicon base and is again referred to as the substrate. As with the depletion-type MOSFET, the substrate is sometimes internally connected to the source terminal, while in other cases a fourth lead is made available for external control of its potential level.

The SiO_2 layer is still present to isolate the gate metallic platform from the region between the drain and source, but now it is simply separated from a section of the p-type material. In summary, therefore, the construction of an enhancement-type MOSFET is quite similar to that of the depletion-type MOSFET, except for the absence of a channel between the drain and source terminals.

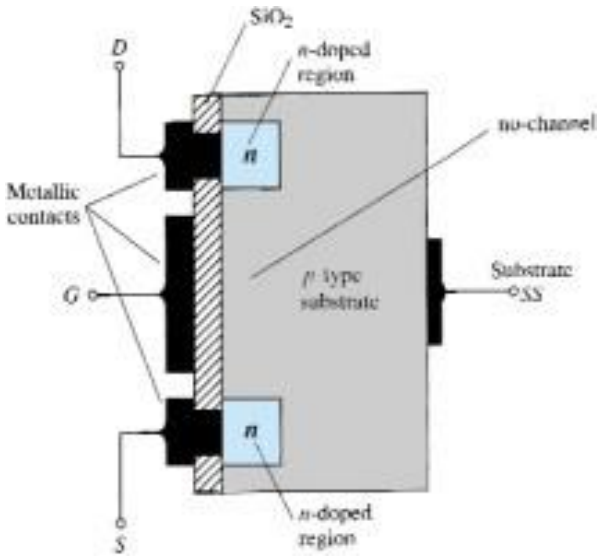


Fig 1. N channel enhancement type MOSFET

Basic Operation and Characteristics

If V_{GS} is set at 0 V and a voltage applied between the drain and source of the device of Fig. 1, the absence of an n-channel (with its generous number of free carriers) will result in a current of effectively zero amperes—quite different from the depletion- type MOSFET and JFET where I_D - I_{DSS}.

It is not sufficient to have a large accumulation of carriers (electrons) at the drain and source (due to the n-doped regions) if a path fails to exist between the two. With VDS some positive voltage, VGS at 0 V, and terminal SS directly connected to the source, there are in fact two reverse-biased p-n junctions between the n-doped regions and the p-substrate to oppose any significant flow between drain and source.

In Fig. 2 both VDS and VGS have been set at some positive voltage greater than 0 V, establishing the drain and gate at a positive potential with respect to the source. The positive potential at the gate will pressure the holes (since like charges repel) in the p-substrate along the edge of the SiO2 layer to leave the area and enter deeper regions of the p-substrate, as shown in the figure.

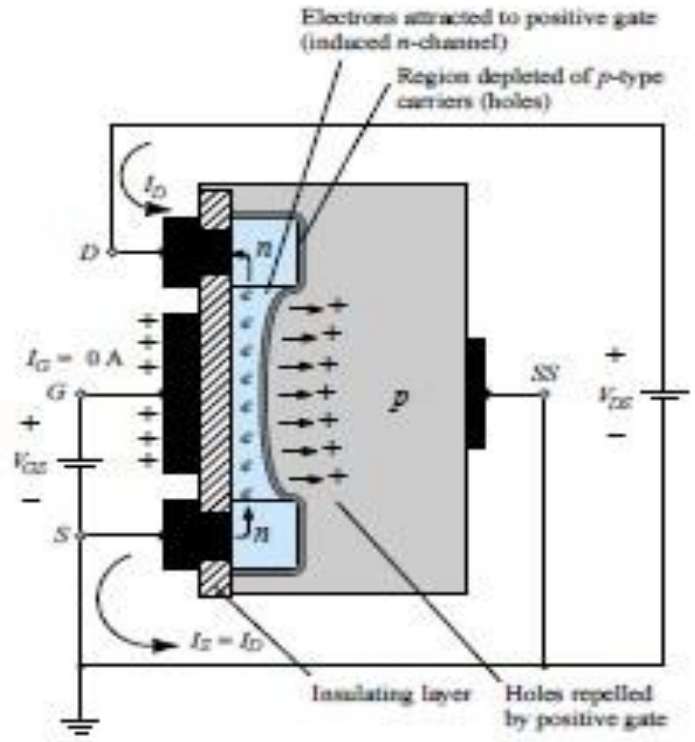


Fig 2. Channel formation

As *VGS* is increased beyond the threshold level, the density of free carriers in the induced channel will increase, resulting in an increased level of drain current. However, if we hold *VGS* constant and increase the level of *VDS*, the drain current will eventually reach a saturation level as occurred for the JFET and depletion-type MOSFET.

The leveling off of I_D is due to a pinching-off process depicted by the narrower channel at the drain end of the induced channel as shown in Fig. 3. Applying Kirchhoff's voltage law to the terminal voltages of the MOSFET of Fig. 3, we find that

$$V_{DG} = V_{DS} - V_{GS}$$

The drain characteristics of Fig. 5.34 reveal that for the device of Fig 3 with VGS = 8 V, saturation occurred at a level of VDS = 6 V. In fact, the saturation level for VDS is related to the level of applied VGS by

$$V_{DSsat} = V_{GS} - V_T$$

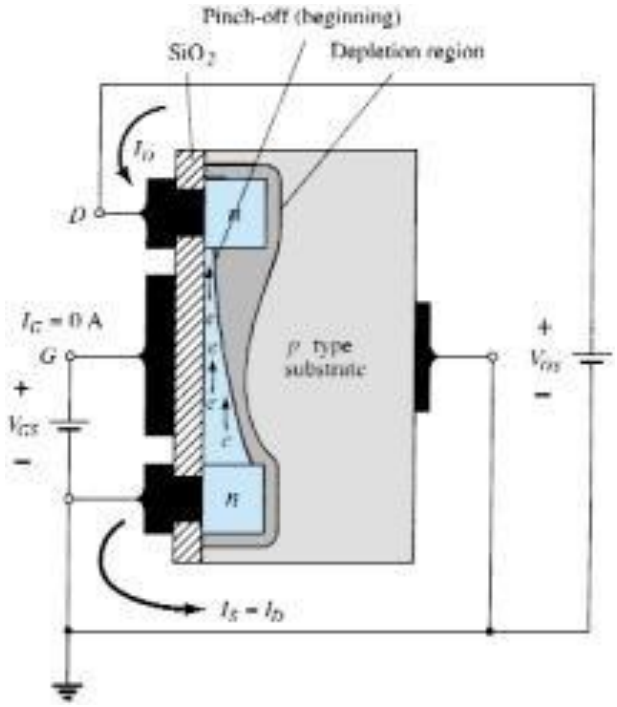


Fig 3. Change in channel and depletion region with increasing V_{DS}

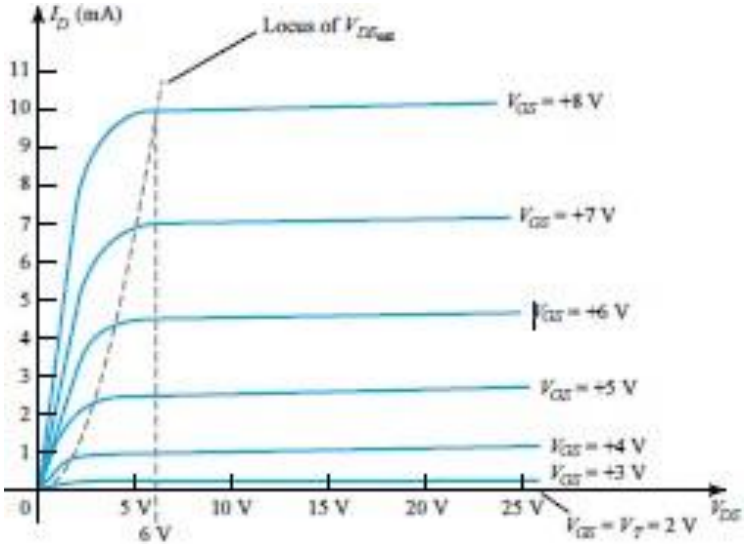


Fig 4. Drain characteristics

For levels of VGS > VT, the drain current is related to the applied gate-to-source voltage by the following nonlinear relationship:

$I_D = k(V_{GS} - V_T)^2$

Again, it is the squared term that results in the nonlinear (curved) relationship between ID and VGS. The k term is a constant that is a function of the construction of the device. The value of k can be determined from the following equation where ID(on) and VGS(on) are the values for each at a particular point on the characteristics of the device.

$$k = \frac{I_{D(on)}}{(V_{GS(on)} - V_T)^2}$$