UNIT IV – SPECIAL SEMICONDUCTOR DEVICES

INTRODUCTION

In addition to the PN – junction diode, other types are also manufactured for specific applications.

METAL – SEMICONDUCTOR JUNCTIONS

Metal – Semiconductor junctions are very common in all semiconductor devices and have very high importance. Depending upon the doping concentration, materials, and the characteristics of the interface, the metal – semiconductor junctions can act as either an ohmic contact or as a Schottky barrier. An analysis of metal – semiconductor is presented.

Structure of Metal – Semiconductor Junction

A metal – semiconductor junction, as the name indicates, consists of a metal in contact with a piece of semiconductor. The structure of a typical metal – semiconductor junction is shown. The active junction is the interface between the metal, which act as an anode, and the semiconductor. The other interface between the semiconductor and metal, which acts as a cathode, is an ohmic contact and there is no potential drop at this junction.

Energy Band Diagram

The energy band diagram helps in identifying the barrier between the metal and the semiconductor. In order to understand the energy band structure at a metal – semiconductor junction, first let us consider the energy bands in metal and semiconductor separately. The energy bands are aligned at the same vacuum level. When the metal and semiconductor are brought together, the Fermi level does align them at thermal equilibrium. The condition that exists before the thermal equilibrium is reached is depicted in the fig below.

Let us define Φ_B, the barrier height as the potential difference between the Fermi level of the metal and the band edge where the majority carriers exist. For an N – type semiconductor, the barrier height id given by the difference between the metal work function (Φ_M) and the electron affinity (χ).

$$\Phi_{BN} = \Phi_M - \chi$$

The work function Φ_M varies depending upon surface preparation. For P – type semiconductor, the barrier height is given by the difference between the valence band and the Fermi level in the metal,

$$\Phi_{BP} = \chi + \frac{E_g}{q} - \Phi_M$$

$$E_g = energy\ gap\ between\ the\ conduction\ and\ valence\ bands.$$

The sum of the barrier heights on N – type and P – type substrate is expected to be equal to the energy gap, $E_g, i.e., (\Phi_{BN} + \Phi_{BP})q = E_g$.

In a metal – semiconductor junction, a barrier is formed if the Fermi level of the metal is somewhere between the valence and conduction band edges of the semiconductor. Let us also define a built – in potential (Φ_1) as the difference between the Fermi level of the metal and the Fermi level of the semiconductor.

For an N – type semiconductor, the barrier height is given by,

$$\Phi_{BN} = \Phi_M - \chi$$

$$\Phi_{IN} = \Phi_{BN} - \frac{E_C - E_F}{q} = \Phi_M - \chi - \frac{E_C - E_F}{q}$$

For an P – type semiconductor, the Fermi level is closer to the valence band and the built – in potential is given by,

$$\Phi_{IP} = \chi + \frac{E_F - E_V}{q} - \Phi_M$$

The Fermi level in an N – type semiconductor is given by

$$E_F = E_C - kTln\frac{N_C}{N_D}$$

and the Fermi level in a P – type semiconductor is given by

$$E_F = E_V + kTln\frac{N_V}{N_A}$$

Substituting the above equations

$$\Phi_{IN} = \Phi_{BN} - \frac{E_C - E_F}{q} = \Phi_{BN} - \frac{kT}{q}ln\frac{N_C}{N_D}\ for\ N - type\ semiconductor$$

$$\Phi_{IP} = \Phi_{BP} - \frac{E_F - E_V}{q} = \Phi_{BP} - \frac{kT}{q}ln\frac{N_V}{N_A}\ for\ P - type\ Semiconductor$$

Thermal Equilibrium

After the metal and semiconductor have been brought into contacts, electrons start to flow from the semiconductor into the metal, and as a result, a depletion region of width x_d, with uncompensated donors is formed. Electrons continue to flow into the metal until the Fermi level of metal and

semiconductor align with each other. In metal, the electron current forms a negative surface charge layer. This result is an electric field and the band edges are lowered in the semiconductor as shown.

Forward and Reverse Bias

When an external bias is applied, the metal – to – semiconductor barrier remains unchanged, whereas, the semiconductor – to – metal barrier is either decreased (forward bias) or increased (reverse bias).

When the metal is connected to a positive bias with respect to the semiconductor. The Fermi energy level of the metal is lowered from its equilibrium level. The depletion region is narrowed, and the potential barrier in the semiconductor is reduced. The number of electrons that diffuse from the semiconductor to metal is now more than the number of electrons that drift from metal into the semiconductor. Thus, there will be positive current through the device.

If the metal is connected to a negative bias with respect to the semiconductor, the metal is charged even more negatively than without any bias. The Fermi energy level of the metal is raised. The electrons in the semiconductor side are repelled even more. The depletion region becomes wider and the potential barrier on semiconductor side is further increased as shown. However, the barrier on the metal side remains unchanged and limits the flow of electrons. A small current flows as a result of a few electrons in the metal acquiring enough thermal energy to overcome barrier.

Ohmic Contacts

An ohmic contact is another type of metal – semiconductor junction. It is formed by applying a metal to a heavily doped semiconductor. Here the current is conducted equally in both directions and there will be a very little voltage drop across the junction. The usage of ohmic contacts is to connect one semiconductor device to another on an IC, or to connect an IC to its external terminals.

Ohmic contacts are very common in semiconductor devices. Metal – semiconductor contacts cannot be considered to offer a resistance as low as that of two metals connected to each other. Metal – semiconductor junction can act as either a rectifying junction or an ohmic contact depending on the Fermi levels of the metal and the semiconductor used. A proper choice of metal and semiconductor can offer a low resistance ohmic contact. Alternatively, the contacts

that have a thin barrier can be created by heavily doping the semiconductor through which the carriers can tunnel. Both these types of contacts are presented.

A metal – semiconductor junction can be an ohmic contact if the Schottky barrier height, $\emptyset_B$ is zero or negative. This means, for an N – type semiconductor, the metal work function, $\emptyset_M$, is either close to or smaller than the electron affinity (χ) of the semiconductor; and for a P – type semiconductor, the metal work function is either close to or greater than the sum of electron affinity and the band gap energy.

That is, $$\phi_M \leq \chi \; for \; an \; N - type \; semiconductor$$

Or, $$\phi_M \geq \chi + E_g \; for \; an \; P - type \; semiconductor$$

Metal-Semiconductor Field Effect Transistor (MESFETs)

MESFET stands for metal–semiconductor field effect transistor. It is quite similar to a JFET in construction and term inology. The difference is that instead of using a p-n junction for a gate, a Schottky (metal-semiconductor) junction is used. MESFETs are usually constructed in compound semiconductor technologies lacking high quality surface passivation such as GaAs, InP, or SiC, and are faster but m ore expensive than silicon-based JFETs or MOSFETs. Production MESFETs are operated up to approximately 45 GHz, and are commonly used for microwave frequency communications an d radar. From a digital circuit design perspe ctive, it is increasingly difficult to use MESFETs as th e basis for digital integrated circuits as the s cale of integration goes up, compared to CMOS silicon based fabrication.

The Metal-Semiconductor-Field-Effect-Transistor (MESFET) consists of a conducting channel positioned between a source and drain contact region as shown in the Figure 1. The carrier flow from source to drain is controlled by a Schottky metal gate. The channel is obtained by varying the deplletion layer width underneath the metal conta ct which modulates the thickness of the conducting ch annel and thereby the current between source and drain.

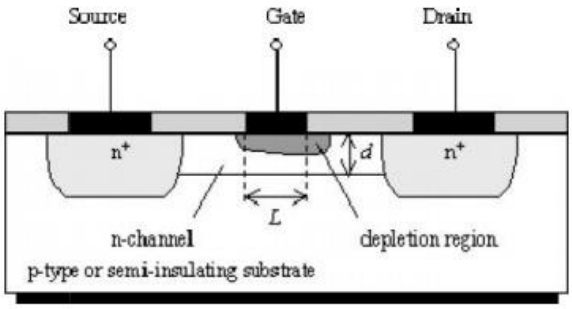


Figure 1 Structure of MESFET

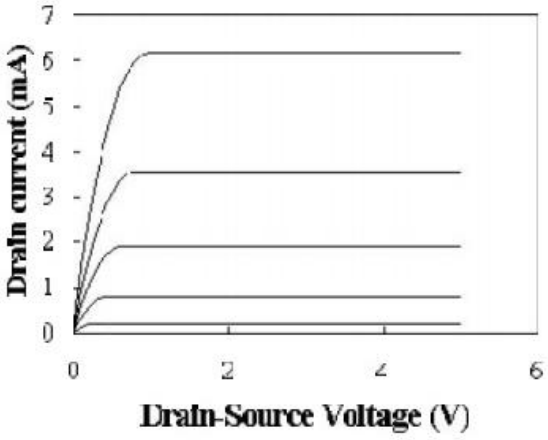


Figure 2 MESFETcharacteristics

Application

Numerous MESFET fabrication possibilities have been explored for a wide variety of semiconductor systems. Some of the main application areas are:

- military communications
- As front end low noise amplifier of microwave receivers in both military radar devices and communication
- commercial optoelectronics
- satellite communications
- As power amplifier for output stage of microwave links.
- As a power oscillator.

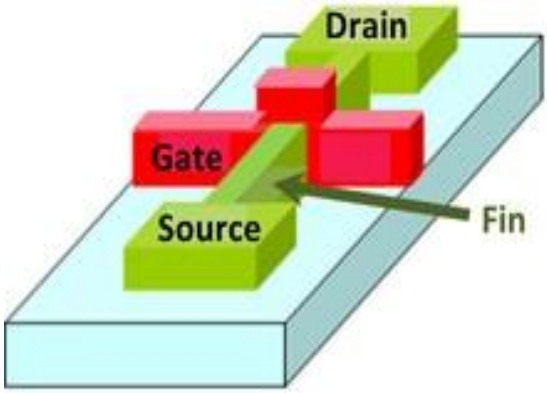
Advantage of the MESFET

- The higher transit frequency of the MESFET makes it particularly of interest for microwave circuits. While the advantage of the MESFET provides a superior microwave amplifier or circuit, the limitation by the diode turn-on is easily tolerated.
- Typically depletion-mode devices are used since they provide a larger current and larger transconductance and the circuits contain only a few transistors, so that threshold is not a limiting factor.
- The buried channel also yields a better noise performance as trapping and release of carriers into and from surface states and defects is eliminated.
- The use of GaAs rather than silicon MESFETs provides two more significant advantages: first, the electron mobility at room temperature is more than 5 times larger, while the peak electron velocity is about twice that of silicon.
- Second, it is possible to fabricate semi-insulating (SI) GaAs substrates, which eliminates the problem of absorbing microwave power in the substrate due to free carrier absorption.

Disadvantage of the MESFET

- The disadvantage of the MESFET structure is the presence of the Schottky metal gate. It limits the forward bias voltage on the gate to the turn-on voltage of the Schottky diode. This turn-on voltage is typically 0.7 V for GaAs Schottky diodes.
- The threshold voltage therefore must be lower than this turn-on voltage. As a result it is more difficult to fabricate circuits containing a large number of enhancement-mode MESFET.

FINFET:



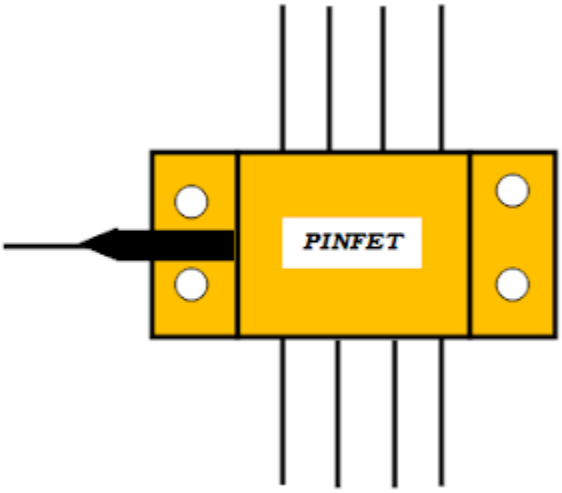
The distinguishing characteristic of the FinFET is that the conducting channel is wrapped by a thin silicon "fin", which forms the body of the device. The thickness of the fin (measured in the direction from source to drain) determines the effective channel length of the device. In current usage the term FinFET has a less precise definition.

Among microprocessor manufacturers, AMD, IBM, and Motorola describe their double-gate development efforts as FinFET[] development whereas Intel avoids using the term to describe their closely related tri-gate architecture. In the technical literature, FinFET is used somewhat generically to describe any fin- based, multigate transistor architecture regardless of number of gates.

A 25-nm transistor operating on just 0.7 volt was demonstrated in December 2002 by Taiwan Semiconductor Manufacturing Company. The "Omega FinFET" design is named after the similarity between the Greek letter omega (Ω) and the shape in which the gate wraps around the source/drain structure. It has a gate delay of just 0.39 picosecond (ps) for the N-type transistor and 0.88 ps for the P-type.

FinFET can also have two electrically independent gates, which gives circuit designers more flexibility to design with efficient, low-power gates.[12]

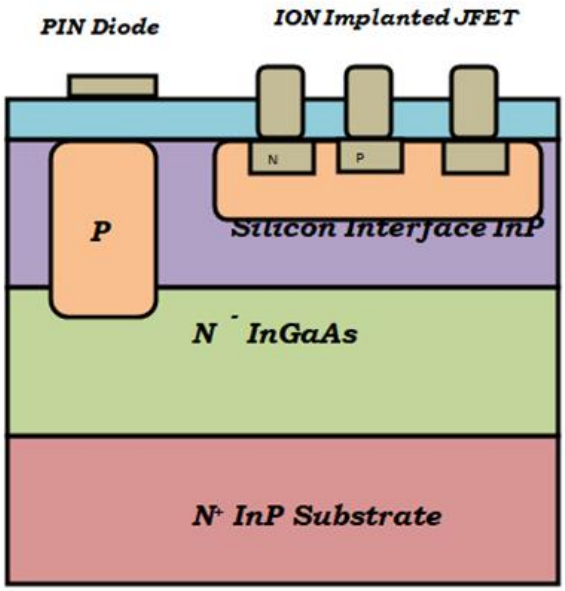
PINFET



PINFET

PINFET stands for P type- intrinsic- N type Field Effect transistor. It is a integration of PIN Photodiode and FET in a single IC. PIN diode converts light energy into an electrical signal and it is designed to operate in a reverse biased condition. Field Effect Transistor is a voltage controlled device. The voltage which is given in the gate terminal as input controls the current passing through it.

Construction of PINFET:



Construction of PINFET

PINFET is the combination of InGaAs PIN Photodiode and InGaAs FET. The construction process includes the following

1) Metal Organic chemical vapour deposition(MOCVD):

By using this method PINFET is fabricated over semi insulating InGaAs substrate.

2) Chloride Vapour Phase epitaxy(VPE):

By this process InGaAs layer of low concentration of electrons is grown above the substrate.

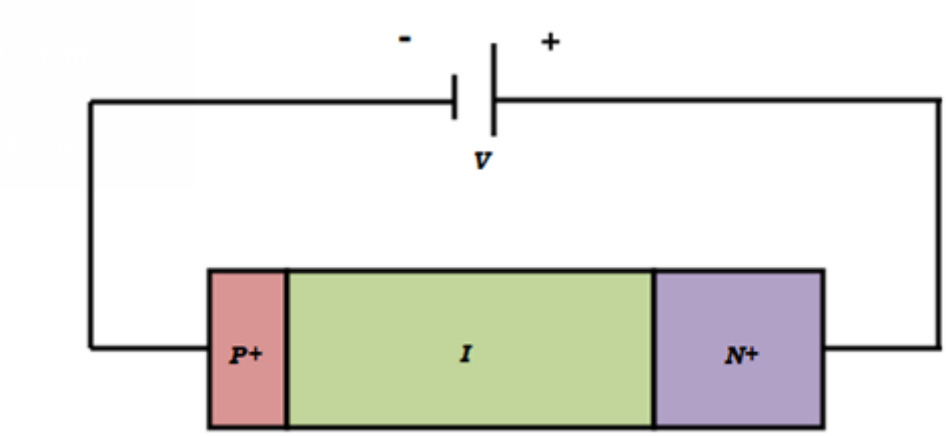
3) Atmospheric pressure metal organic chemical vapour deposition technique:

By this method silicon interface layer is grown over the InGaAs layer.

4) Ion Implantation: By this process which is done in series the FET is formed.

5) Deposition and diffusion: By this process PIN diode is formed.

Working of PINFET:



Working of PINFET

It consists of three regions P region, I region and N region. P region and N region are heavily doped regions and they are used as Ohmic contacts. A wider intrinsic silicon layer is sandwiched between two heavily doped layers and it absorbs the light photons which forms the electron hole pairs. The intrinsic layer is highly resistive and it increases the width of the depletion

region. In normal diode only voltage is used to form the current but in PINFET both voltage and light is used to form the current.

When reversed biased the majority carriers in highly doped P type and N type does not conduct current so the charge carriers move away from the junction and the intrinsic layer is undoped which does not have majority charge carriers. So the width of the depletion region increases. When the light is incident on the PINFET the wider intrinsic layer absorbs the light energy and forms large number of electron hole pairs.

The free electrons which are generated in the intrinsic region move towards the N region and the free holes move towards the P region and these charge carriers are attracted towards the positive and negative terminals. Thus current is formed due to the movement of these charge carriers.

The intrinsic layer acts as a dielectric layer and highly doped P and N layer acts as electrodes in the capacitor. Since the distance between the electrodes are very large, the capacitance is very low and thus the noise is very low.

Advantages of PINFET:

- Wide bandwidth
- Low noise
- High sensitivity to light
- Low sensitivity to temperature
- Low cost
- Small size
- Long lifetime

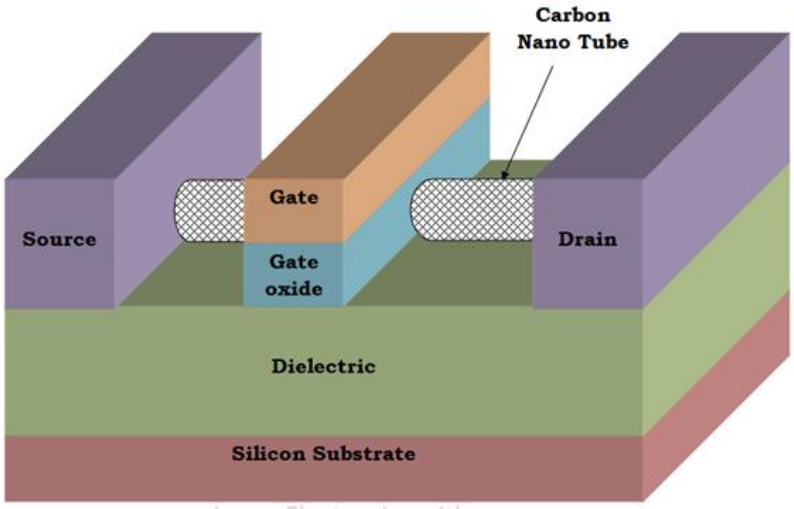
Disadvantages of PINFET:

- It always operates in reverse biased condition
- It is a light sensitive device
- Should not exceed the working temperature limit specified by the manufacturer.

Applications

- PINFET is mainly used as a photo receiver in optical communication because of its low noise and high speed.
- Used in optical Sensor systems.
- Used as repeaters in telecommunication

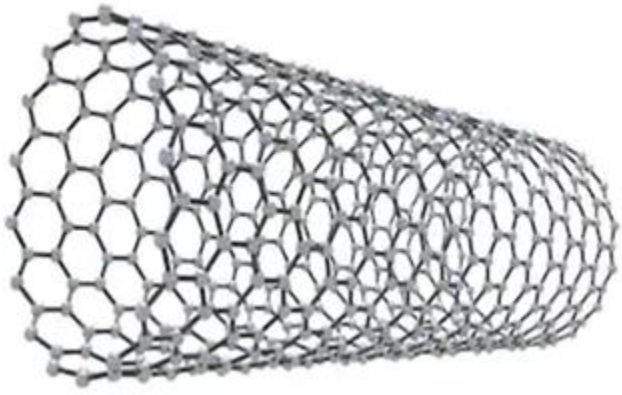
CNTFET



Carbon Nano Tube Field Effect Transistor

CNTFET stands Carbon Nano Tube Field Effect Transistor. CNTFET is a FET which uses Carbon Nano Tube as the channel. They are widely used in many applications because of their both metallic and semiconductor properties and because of their ability to carry high current. In new technology advancement there is a demand of integrated circuits with high speed performance, low power consumption and smaller dimension. The size of the transistor had reduced as per the Moore's law but there are some disadvantages like shorter channel effect which leads to direct tunnelling, increase in gate leakage current. This disadvantages are overcome by CNTFET.

What is Carbon Nano Tube?



Carbon Nano Tube

Carbon Nano tubes were first discovered by Sumio Iijima in the year 1991. These nano tubes consist of carbon atoms with diameters measured in nano metres which are linked in hexagonal shape. Each carbon atom is covalently bonded to other three atoms. The width of the carbon nanotubes are of 1nm and length maybe some centimetres. Though they are very small they are strong and not brittle or fragile. They can be bent and when released they go back to their original shape.

There are two types

1) Single-walled and its diameter is of 1nm and

2) Multi-walled in which many layers are interlinked and its diameter is of 100nm.

Carbon nano tubes are formed by rolling either single walled sheet of graphene or multi walled sheet of graphene. In graphene the carbon atoms are arranged in two dimensional honeycomb lattices. The Carbon nano tubes are made by three methods arc discharge, laser ablation of graphite and chemical vapour deposition (CVD).

Types of CNTFET:

Based on Geometry it is classified into

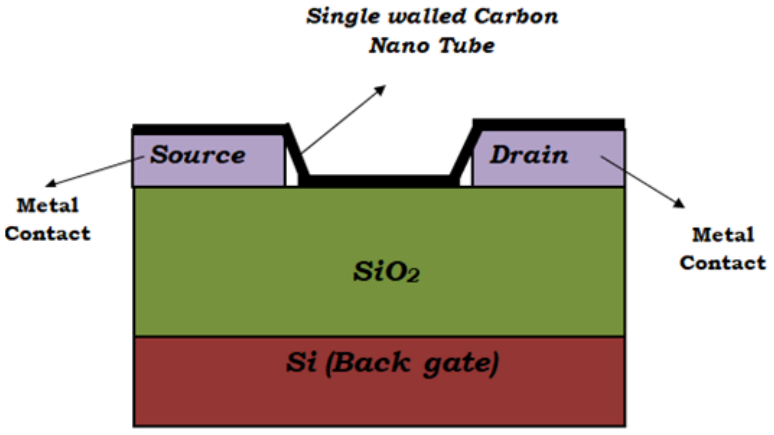
1) Back gate CNTFET

2) Top gate CNTFET

3) Wrap- around gate CNTFETs

4) Suspended CNTFETs

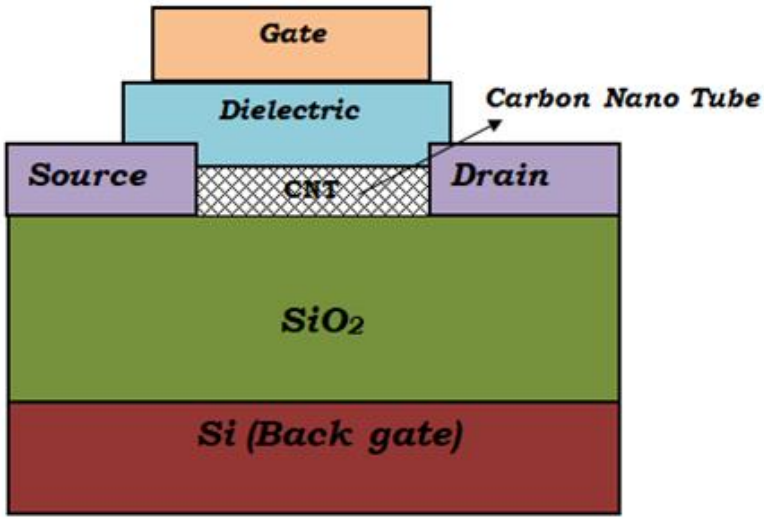
1) Back gate CNTFET:



Back Gate CNTFET

In this method during the earlier stage of manufacturing, Silicon dioxide (SiO2) layer is fabricated above the silicon layer. Silicon dioxide is the gate oxide above which a single walled carbon nano tube (SWCNT) is bridged between two metal pre fabricated strip on the silicon dioxide layer by lithography. One metal is source and the other is drain. The CNT is randomly placed above the metal strips. The limitation of this model are high parasitic contact resistance, low drive currents and low transconductance. To overcome these limitations next generation CNTFET is developed.

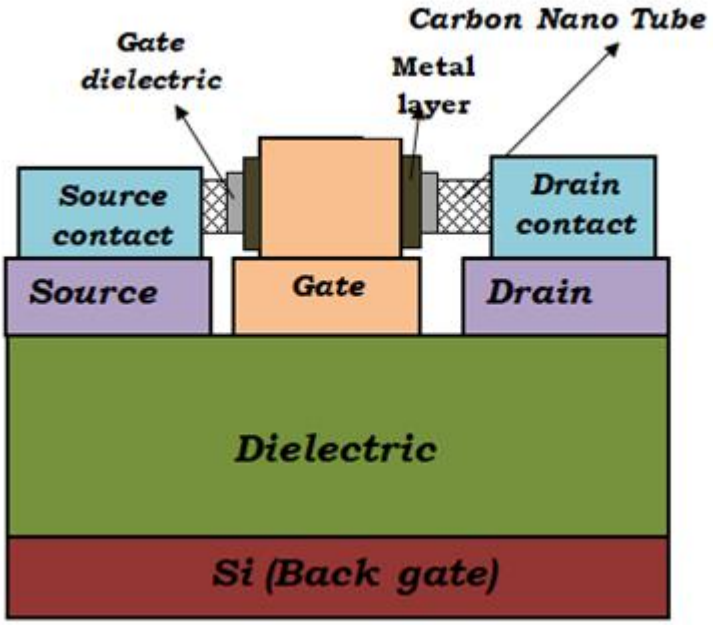
2) Top gate CNTFET:



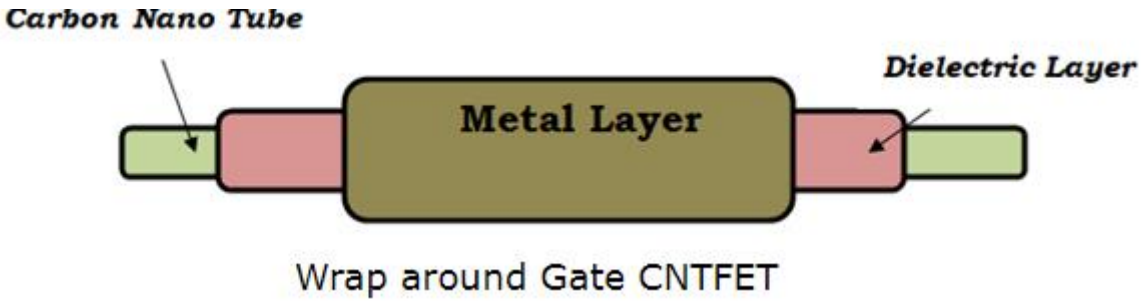
Top Gate CNTFET

In this model as the name says the gate is fabricated over the Carbon Nano Tubes. The source and the drain are patterned by high resolution electron beam lithography. A layer of dielectric is fabricated above the carbon tube by evaporation or atomic layer deposition. Many top gate CNTFET can be fabricated on a same wafer on which the gates are electrically isolated. The advantage of this method is drain current is increased from nanometers to micrometers, trans conductance is also increased. So this method is preferred over the previous method though the fabrication process is complex.

3) Wrap- around gate CNTFETs



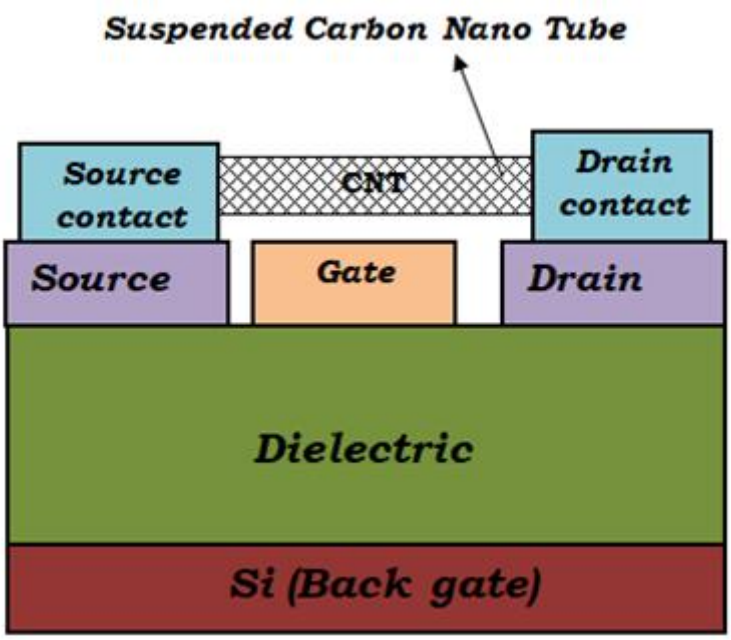
Wrap around Gate CNTFET



Wrap around Gate CNTFET

Wrap around CNTFET is also known as gate – all – around CNTFET and it was developed in the year 2008. In other methods only part of the nanotubes is gated. Here the entire nano tube is covered by gate which reduces leakage current and it improves the electrical performance. The fabrication process starts by wrapping the carbon nano tube with dielectric layer by atomic layer deposition. The wrapping is partially etched to expose the ends of the nanotube. Then the source, drain and gate contacts are deposited on the nanotubes.

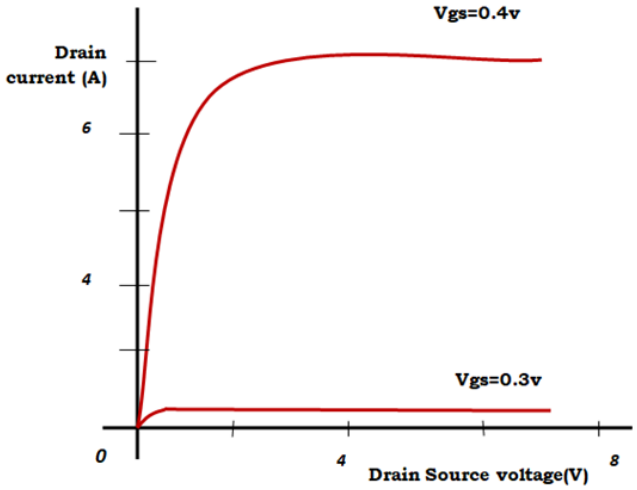
4) Suspended CNTFETs



Suspended CNTFET

In this method gate is suspended over a trench to reduce the contact with substrate and gate oxide. Thus the device performance is increased. But the drawback in this method is gate electric is air or vacuum. Only short CNTs are used because long tubes may touch the metal contact which may short the device. It is not available commercially. It used to research about the intrinsic properties of clean CNT.

I-V characteristics of CNTFET:



I-V Characteristics of CNTFET

Initially when the applied voltage is below the threshold voltage the drain current is almost zero. When it crosses the threshold voltage the drain current increases gradually.

The current generated depends upon the Schottky barrier formed at the junction of CNT and the metal contact at source and the drain. The metals used here are silver, titanium, palladium and aluminium.

Comparison of CNTFET with MOSFET:

1) In MOSFET switching occurs by altering channel resistivity in CNTFET switching occurs by modulation of contact resistance.
2) CNTFET generates three to four times of drive current than MOSFET.
3) Transconductance of CNTFET is four times higher than the MOSFET.
4) The average carrier velocity is double in CNTFET than that is in MOSFET.

Advantages

- Low power consumption
- Electron mobility is high
- Lower threshold voltages
- Better control over channel formation
- No direct tunneling
- Gate leakage current is reduce

Disadvantages

- Cannot be operated at high temperature or at high electric current.
- Lifespan is less.
- Fabrication process is difficult.
- Cost of production is high.

Applications

- Used in solar cell
- Used mainly in VLSI
- Used in faster computer chips
- Cancer treatment
- Cardiac autonomic regulation
- For platelet activation
- For tissue regeneration