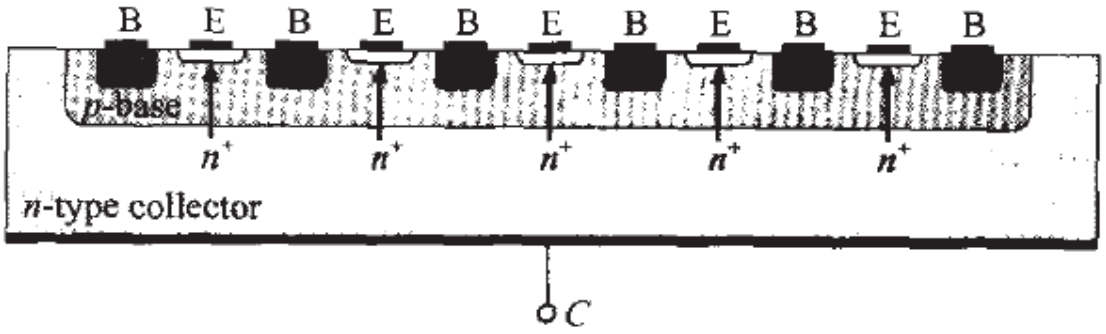
5.5 BIPOLAR JUNCTION TRANSISTORS:

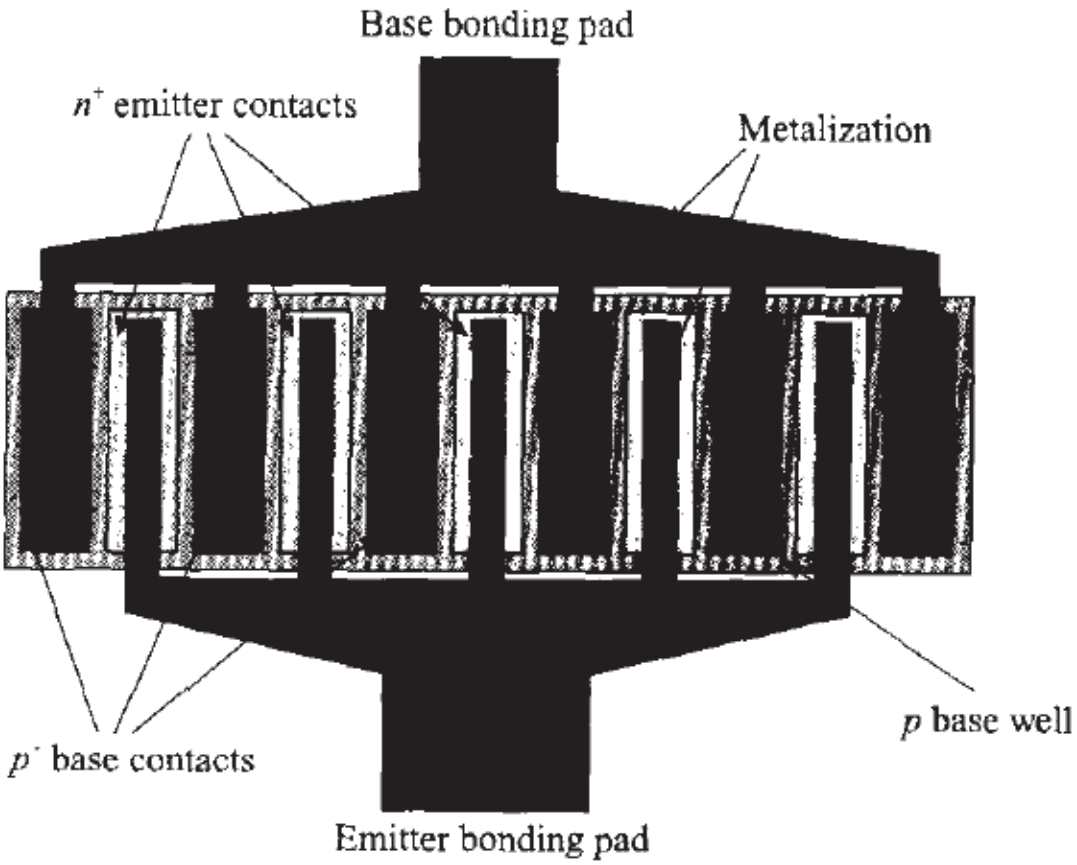
The constituents of a bipolar junction transistor are three alternatively doped semiconductors, in pnp on npn configuration. As the word bipolar means, the internal current is due to both minority and majority carriers.

The BJT is one of the widely used active RF elements due to its low-cost construction, relatively high operating frequency, low noise performance, and high-power handing capacity. The high-power capacity is achieved through a special inter-digital emitter-base construction as a part of planer structure. Figure 5.6.1(a), shows both the cross-sectional planer construction and the top view of an interdigital emitter-base connection.

Because of the interleaved construction shown in Figure 5.6.1 (b) the base-emitter resistance is kept at a minimum while not compromising the gain performance. A low base resistance directly improves the signal-to-noise ratio by reducing the current density through the base emitter junction and by reducing the random thermal motion in the base.



(a) Cross-sectional view of a multifinger bipolar junction transistor



(b) Top view of a multifinger bipolar junction transistor

Figure 5.6.1 Interdigitated structure oh high-frequency BJT

[Source: Reinhold Ludwig and Powel Bretchko,‖ RF Circuit Design – Theory and Applications, Page-313]

The BJT is still the preferred device in very demanding analog circuit applications, both integrated and discrete. This is especially true in very-high-frequency applications, such as radio frequency (RF) circuits for wireless systems. A very-high-speed digital logic-circuit family based on bipolar transistors, namely emitter-coupled logic, is still in use. Finally, bipolar transistors can be combined with MOSFETs to create innovative circuits that take advantage of the high-input-impedance and low-power operation of MOSFETs and the very-high-frequency operation and high-current-driving capability of bipolar transistors. The resulting

technology is known as BiMOS or BiCMOS. Fig 5.6.2 shoes a cross-sectional view of such a structure.

The bipolar transistor enjoyed nearly three decades as the device of choice in the design of both discrete and integrated circuits. Although the MOSFET had been known very early on, it was not until the 1970s and 1980s that it became a serious competitor to the BJT. At the time of this writing (2003), the MOSFET is undoubtedly the most widely used electronic device, and CMOS technology is the technology of choice in the design of integrated circuits. Nevertheless, the BJT remains a significant device that excels in certain applications.

A terminal is connected to each of the three semiconductor regions of a transistor, with the terminals labeled emitter (E), base (B), and collector (C). The transistor consists of two pn junctions, the emitter–base junction (EBJ) and the collector–base junction (CBJ). Depending on the bias condition (forward or reverse) of each of these junctions, different modes of operation of the BJT are obtained, as shown in Table 5.1. The active mode, which is also called forward active mode, is the one used if the transistor is to operate as an amplifier. Switching applications (e.g., logic circuits) utilize both the cutoff and the saturation modes.

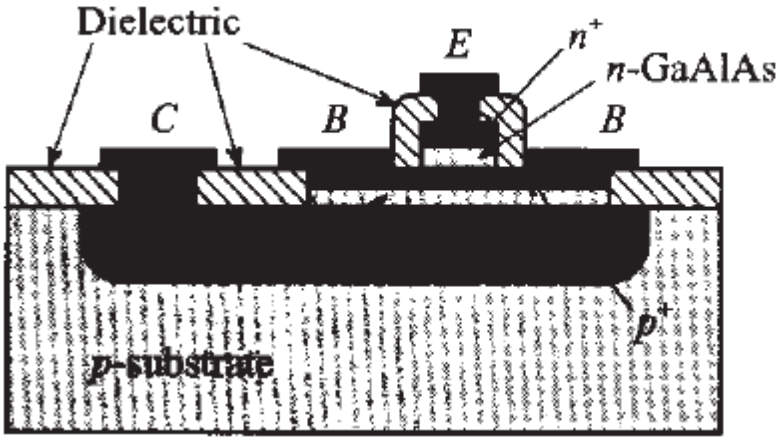


Figure: 5.6.2 Cross-sectional view of a GaAs hetrojunction bipolar junction involving a GaAIAs- GaAs interface

[Source: Reinhold Ludwig and Powel Bretchko,‖ RF Circuit Design – Theory and Applications, Page-314]

The reverse active (or inverse active) mode has very limited application but is conceptually important. As we will see shortly, charge carriers of both polarities—that is, electrons and holes— participate in the current conduction process in a bipolar transistor, which is the reason for the name bipolar. Fig 5.12 shows the cross-sectional view of such a structure.

The forward bias on the emitter–base junction will cause current to flow across this junction. Current will consist of two components: electrons injected from the emitter into the base, and holes injected from the base into the emitter. As will become apparent shortly, it is highly desirable to have the first component (electrons from emitter to base) at a much higher level than the second component (holes from base to emitter). This can be accomplished by fabricating the device with a heavily doped emitter and a lightly doped base; that is, the device is designed to have a high density of electrons in the emitter and a low density of holes in the base. The BJT is a current controlled device that is best explained by referring to Fig 5.6.3(a) which shows the structure, electrical symbol, and diode model with associated voltage and current convention for the npn structure.

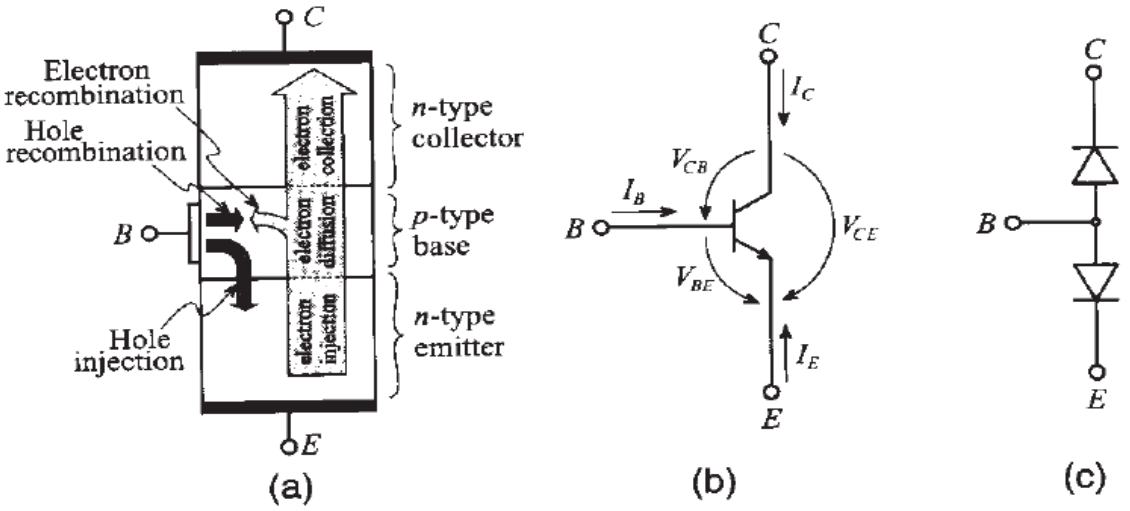
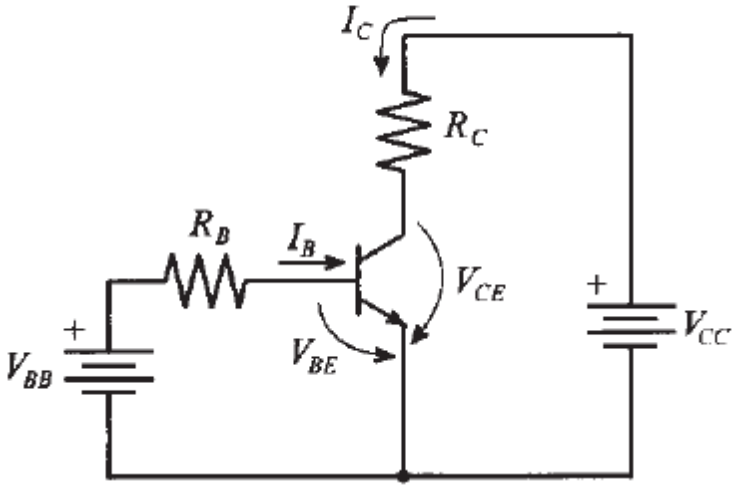


Figure: 5.6.3 npn transistor: (a) structure with electrical charge flow under forward active mode of operation, (b) transistor symbol with voltage and current directions, and (c) diode model.

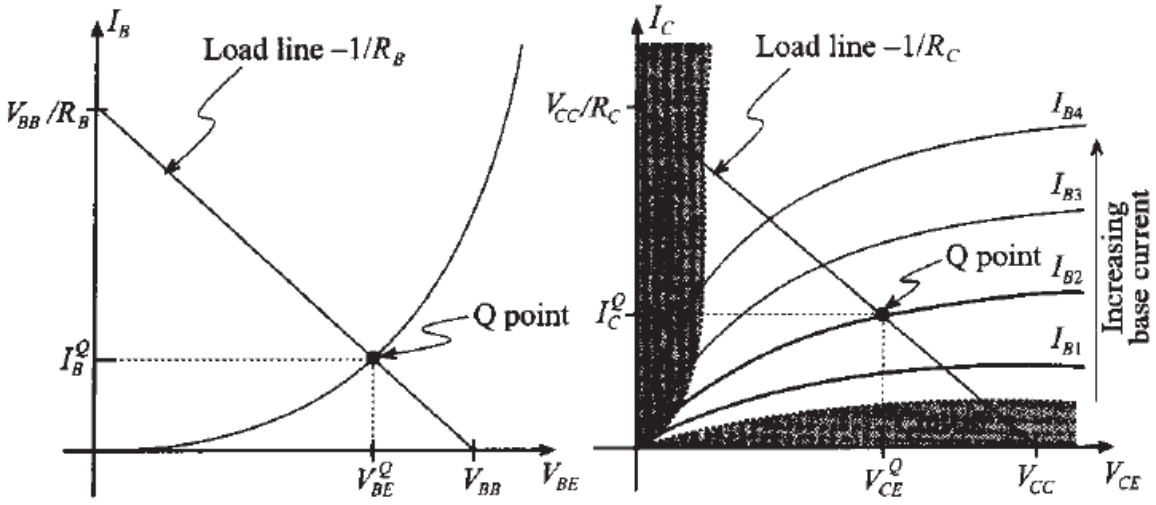
[Source: Reinhold Ludwig and Powel Bretchko,‖ RF Circuit Design – Theory and Applications, Page-315]

Let us now consider the electrons injected from the emitter into the base. These electrons will be minority carriers in the p-type base region. Because the base is usually very thin, in the steady state the excess minority carrier (electron) concentration in the base will have an almost straight-line profile, as indicated by the solid straight line in Fig. 5.6.3(b). The electron concentration will be highest [denoted by np(0)] at the emitter side and lowest (zero) at the collector side.2 As in the case of any forward-biased pn junction (Section 3.X), the concentration will be proportional to $e^{\frac{V_{BE}}{V_\tau}}$ in Fig 5.6.3(c).

$$\boldsymbol{n_P\,(0) = n_{P\,0} e^{\frac{V_{BE}}{V_\tau}}}$$



(a) Biasing circuit for npn BJT in common-emitter configuration



(b) Input characteristic of transistor **(c) Output characteristics of transistor**

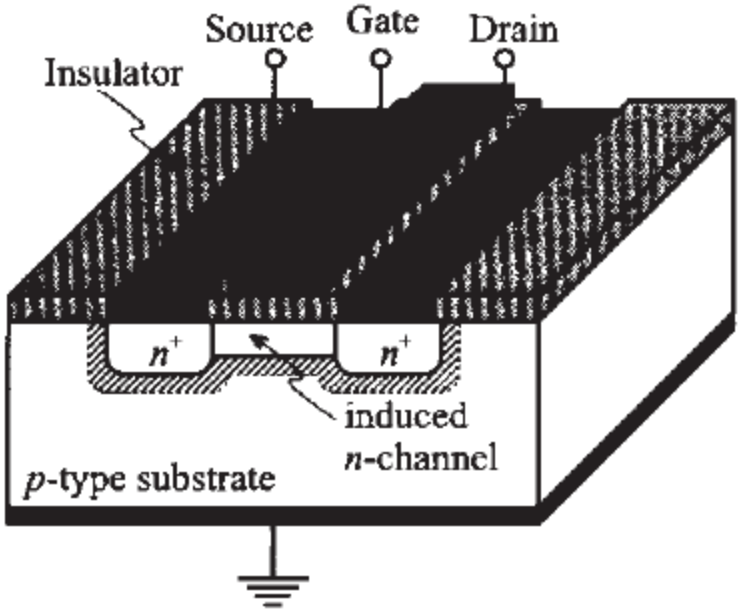
Fig: 5.6.4 Biasing of input, output characteristics of an npn BJT.

[Source: Reinhold Ludwig and Powel Bretchko,‖ RF Circuit Design – Theory and Applications, Page-316]

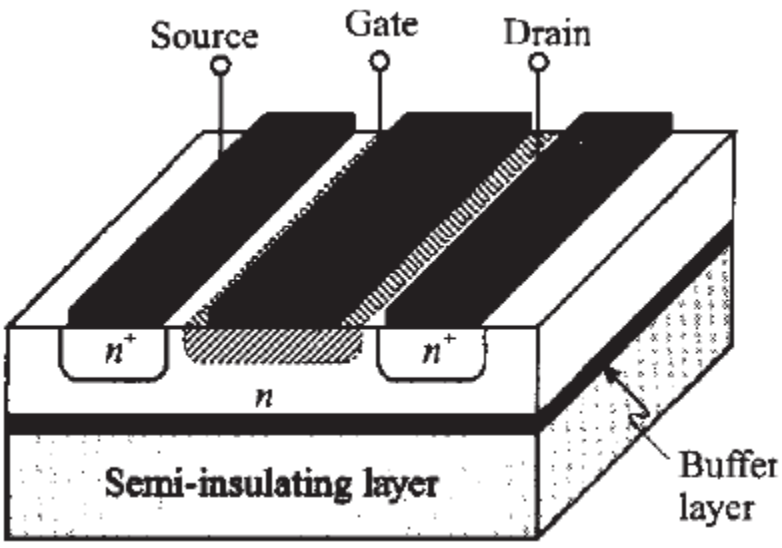
In Fig 5.6.4(a), The saturation current IS is inversely proportional to the base width W and is directly proportional to the area of the EBJ. Typically IS is in the range of 10−12 A to 10−15 A (depending on the size of the device). Because IS is proportional to it is a strong function of temperature, approximately doubling for every 5°C rise in temperature shown in Fig 5.6.4(b). (For the dependence of on temperature) Since IS is directly proportional to the junction area (i.e., the device size), it will also be referred to as the scale current. Two transistors that are identical except that one has an EBJ area, say, twice that of the other will have saturation currents with that same ratio (i.e., 2). Thus for the same value of vBE the larger device will have a collector current twice that in the smaller device. This concept is frequently employed in integrated-circuit design shown in Fig 5.6.4 (c) .

RF FIELD EFFECT TRANSISTORS:

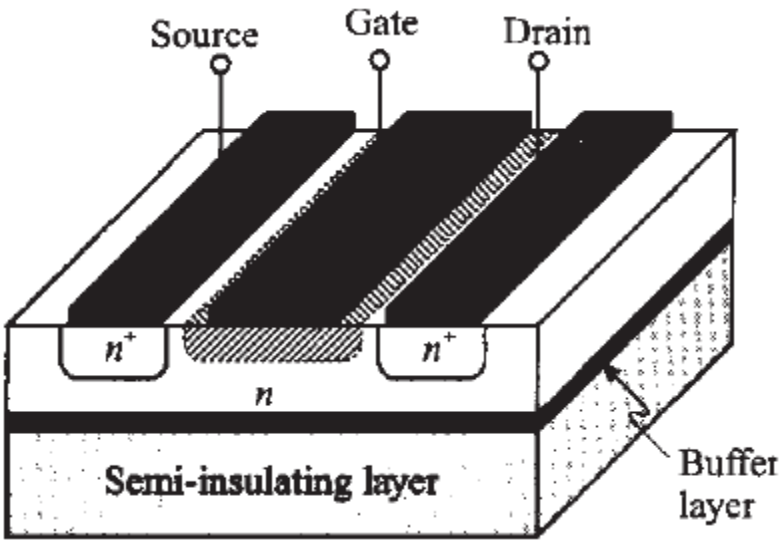
There are two types of field-effect transistors, the Junction Field-Effect Transistor (JFET) and the "Metal-Oxide Semiconductor" Field-Effect Transistor (MOSFET), or Insulated-Gate Field-Effect Transistor (IGFET). The principles on which these devices operate (current controlled by an electric field) are very similar — the primary difference being in the methods by which the control element is made shown in Fig 5.6.5(a)



(a) Metal insulator semiconductor FET (MISFET)



(b) Junction field effect transistor (JFET)



(c) Metal semiconductor FET(MESFET)

Fig : 5.6.5 Construction of a (a) MISFET (b) JFET (c) MESFET

[Source: Reinhold Ludwig and Powel Bretchko,‖ RF Circuit Design – Theory and Applications, Page-330]

MOSFET CAPACITANCES The physical structure of a MOSFET results in capacitors between the terminals. The metal anode gate structure determines the capacitors from gate–to–drain (Cgd), and gate– to–source (Cgs) shown in Fig 5.6.5 (b)

. The PN junction formed during the fabrication of the MOSFET results in a junction capacitance from drain–to–source (Cds). These capacitances are characterized as input (Ciss), output (Coss) and reverse transfer (Crss) capacitances on data sheets. The relationships between the inter–terminal capacitances and those given on data sheets are shown in Fig 5.6.5(c). The Ciss can be specified in two ways: 1. Drain shorted to source and positive voltage at the gate. 2. Positive voltage of the drain in respect to source and zero volts at the gate. In the latter case the numbers are lower.

However, neither method represents the actual operating conditions in RF applications.

DRAIN CHARACTERISTICS One figure of merit for a FET is its static resistance in the full–on condition. This on–resistance, VDS(on), occurs in the linear region of the output characteristic and is specified under specific test conditions for gate–source voltage and drain current. For MOSFETs, VDS(on) has a positive temperature coefficient and constitutes an important design consideration at high temperatures, because it contributes to the power dissipation within the device.

GATE CHARACTERISTICS The gate of the MOSFET is a polysilicon material, and is electrically isolated from the source by a layer of oxide. The input resistance is very high — on the order of 109 ohms — resulting in a leakage current of a few nanoamperes. Gate control is achieved by applying a positive voltage slightly in excess of the gate–to–source threshold voltage, VGS(th)

Gate Voltage Rating — Never exceed the gate voltage rating. Exceeding the rated VGS can result in permanent damage to the oxide layer in the gate region. Gate Termination — The gate of this device is essentially capacitor. Circuits that leave the gate open–circuited or float ing should be avoided. These conditions can result in turn– on of the device due to voltage build–up on the input capacitor due to leakage currents or pickup. Gate Protection — This device does not have an internal monolithic zener diode from gate–to–source shown in in Fig 5.6.5(b).

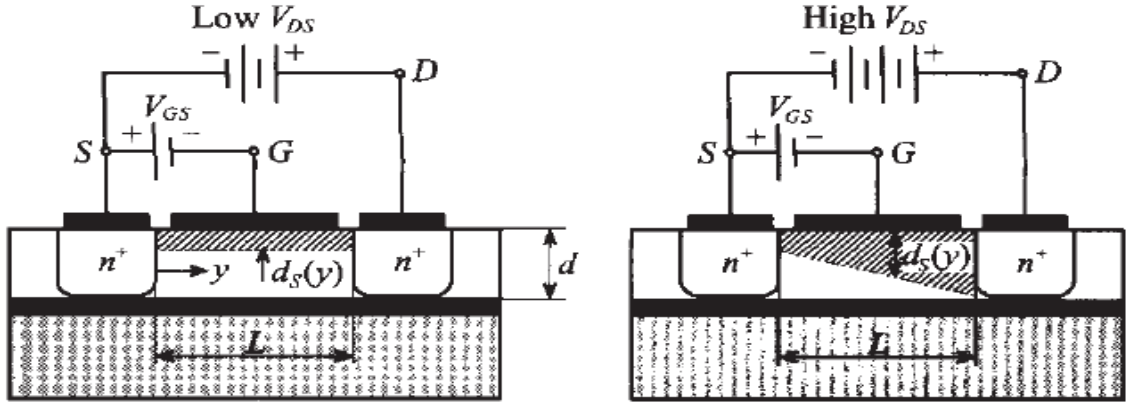
If gate protection is required, an external zener diode is recommended. Using a resistor to keep the gate–to–source impedance low also helps damp transients and serves another important function. Voltage transients on the drain can be coupled to the gate through the parasitic gate–drain capacitance. If the gate–to–source impedance and the rate of voltage change on the drain are both high, then the signal

coupled to the gate may be large enough to exceed the gate–threshold voltage and turn the device on. HANDLING CONSIDERATIONS When shipping, the devices should be transported only in antistatic bags or conductive foam. Upon removal from the packaging, careful handling procedures should be adhered to. Those handling the devices should wear grounding straps and devices not in the antistatic packaging should be kept in metal tote bins. MOSFETs should be handled by the case and not by the leads, and when testing the device, all leads should make good electrical contact before voltage is applied. As a final note, when placing the FET into the system it is designed for, soldering should be done with a grounded iron. DESIGN CONSIDERATIONS The MRF141G is an RF Power, MOS, N–channel enhancement mode field–effect transistor (FET) designed for HF and VHF power amplifier applications. Motorola Application Note AN211A, FETs in Theory and Practice, is suggested reading for those not familiar with the construction and characteristics of FETs. The major advantages of RF power MOSFETs include high gain, low noise, simple bias systems, relative immunity from thermal runaway, and the ability to withstand severely mismatched loads without suffering damage. Power output can be varied over a wide range with a low power dc control signal. DC BIAS The MRF141G is an enhancement mode FET and, therefore, does not conduct when drain voltage is applied. Drain current flows when a positive voltage is applied to the gate. RF power FETs require forward bias for optimum performance. The value of quiescent drain current (IDQ) is not critical for many applications. The MRF141G was characterized at IDQ = 250 mA, each side, which is the suggested minimum value of IDQ. For special applications such as linear amplification, IDQ may have to be selected to optimize the critical parameters. The gate is a dc open circuit and draws no current. Therefore, the gate bias circuit may be just a simple resistive divider network. Some applications may require a more elaborate bias sytem. GAIN CONTROL Power output of the MRF141G may be controlled from its rated value

down to zero (negative gain) by varying the dc gate voltage. This feature facilitates the design of manual gain control, AGC/ALC and modulation systems.

FUCTIONALITY:

The input resistance of the MOSFET is exceptionally high because the gate behaves as a capacitor with very low leakage (rin ≈ 1014 Ω). The output impedance is a function of rds (which is related to the gate voltage) and the drain and source bulk resistances (RD and RS). To turn the MOSFET "on", the gate-channel capacitance, Cg(ch), and the Miller capacitance, Cgd, must be charged. In turning "on", the drain-substrate capacitance, Cd(sub), must be discharged. The resistance of the substrate determines the peak discharge current for this capacitance. The FET just described is called an enhancement-type MOSFET. A depletion-type MOSFET can be made in the following manner: Starting with the basic structure of Figure 4, a moderate resistivity n-channel is diffused between the source and drain so that drain current can flow when the gate potential is at zero volts (Figure 5.6. In this manner, the MOSFET can be made to exhibit depletion characteristics. For positive gate voltages, the structure enhances in the same manner as the device of Figure 5.6.5(b). With negative gate voltage, the enhancement process is reversed and the channel begins to deplete of carriers as seen in Figure 5.6. As with the JFET, drain-current.



(a) Operation in the linear region (b) Operation in the saturation region

Fig : 5.17 Functionality of MSEFET for different drain source voltages

[Source: Reinhold Ludwig and Powel Bretchko,‖ RF Circuit Design – Theory and Applications, Page-331]

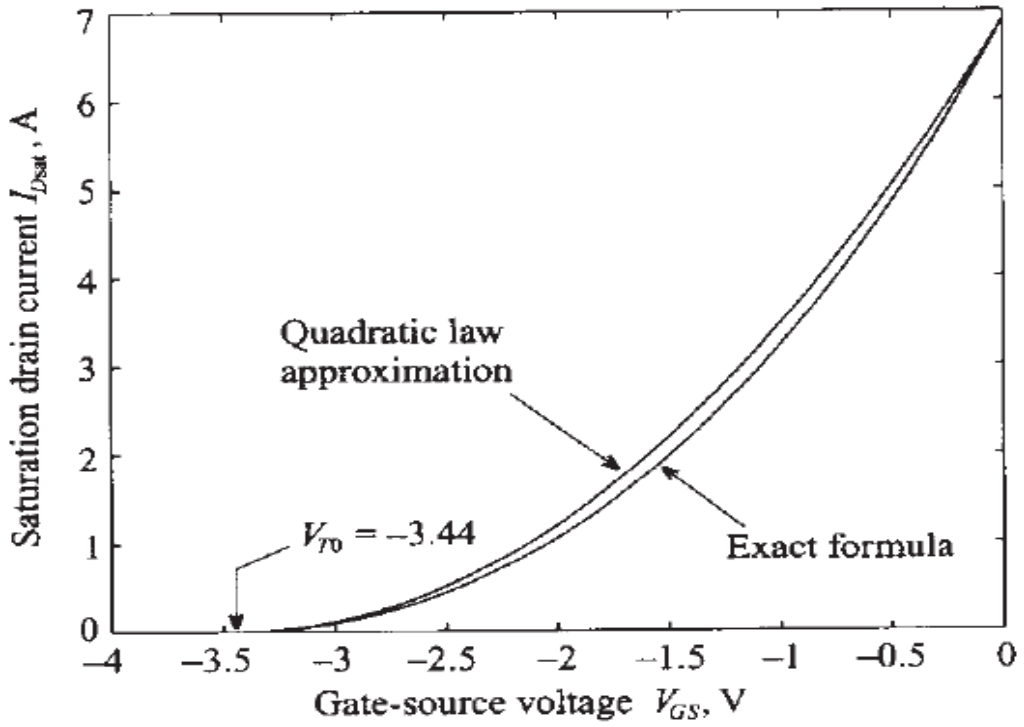


Fig: 5.18 Drain current vs V_{GS}

[Source: Reinhold Ludwig and Powel Bretchko,‖ RF Circuit Design – Theory and Applications, Page-334]