

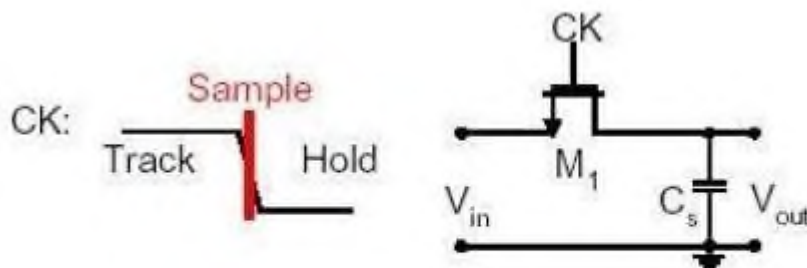
High Speed Sample and Hold Circuits

Introduction:

Sample-and-hold (S/H) is an important analog building block with many applications, including analog-to-digital converters (ADCs) and switched-capacitor filters. The function of the S/H circuit is to sample an analog input signal and hold this value over a certain length of time for subsequent processing.

Taking advantages of the excellent properties of MOS capacitors and switches, traditional switched capacitor techniques can be used to realize different S/H circuits [1]. The simplest S/H circuit in MOS technology is shown in Figure 1, where V_{in} is the input signal, M_1 is an MOS transistor operating as the sampling switch, C_h is the hold capacitor, ck is the clock signal, and V_{out} is the resulting sample-and-hold output signal.

As depicted by Figure 4., in the simplest sense, a S/H circuit can be achieved using only one MOS transistor and one capacitor. The operation of this circuit is very straightforward.



Simplest sample-and-hold circuits in MOS technology.

Figure 4, in the simplest sense, a S/H circuit can be achieved using only one MOS transistor and one capacitor. The operation of this circuit is very straightforward. Whenever ck is high, the MOS switch is on, which in turn allows V_{out} to track V_{in} . On the other hand, when ck is low, the MOS switch is off. During this time, C_h will keep V_{out} equal to the value of V_{in} at the instance when ck goes low.

Unfortunately, in reality, the performance of this S/H circuit is not as ideal as described above. The two major types of errors occur. They are charge injection and clock feed through, that are associated with this S/H implementation. Three new S/H techniques, all of which try to minimize the errors caused by charge injection and/or clock feed through.

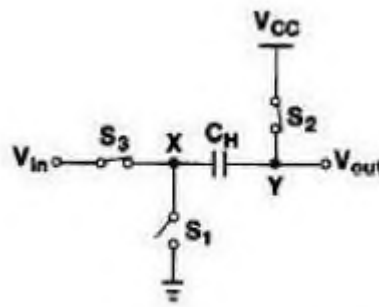
Alternative CMOS Sample-and-Hold Circuits

Three alternative CMOS S/H circuits that are developed with the intention to minimize charge injection and/or clock feed through are

Series Sampling:

The S/H circuit of Figure 4. is classified as parallel sampling because the hold capacitor is in parallel with the signal. In parallel sampling, the input and the output are dc-coupled. On the

other hand, the S/H circuit shown in Figure 2 is referred to as series sampling because the hold capacitor is in series with the signal.



Series sampling.

When the circuit is in sample mode, both switches S_2 and S_3 are on, while S_1 is off. Then, S_2 is turned off first, which means V_{out} is equal to V_{CC} (or V_{DD} for most circuits) and the voltage drop across C_H will be $V_{CC} - V_{in}$. Subsequently, S_3 is turned off and S_1 is turned on simultaneously. By grounding node X , V_{out} is now equal to $V_{CC} - V_{in}$, and the drop from V_{CC} to $V_{CC} - V_{in}$ is equal to the instantaneous value of the input.

As a result, this is actually an inverted S/H circuit, which requires inversion of the signal at a later stage. Since the hold capacitor is in series with the signal, series sampling can isolate the common-mode levels of the input and the output.

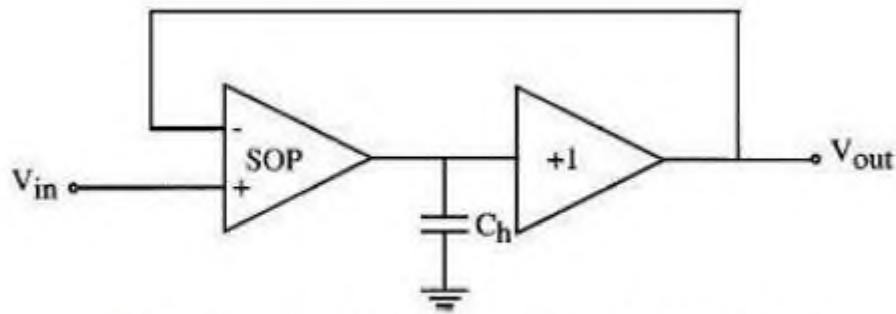
This is one advantage of series sampling over parallel sampling. In addition, unlike parallel sampling, which suffers from signal-dependent charge injection, series sampling does not exhibit such behavior because S_2 is turned off before S_3 . Thus, the fact that the gate-to-source voltage, V_{GS} , of S_2 is constant means that charge injection coming from S_2 is also constant (as opposed to being signal-dependent), which means this error can be easily eliminated through differential operation.

Limitations:

On the other hand, series sampling suffers from the nonlinearity of the parasitic capacitance at node Y . This parasitic capacitance introduces distortion to the sample-and-hold value, thus mandating that C_H be much larger than the parasitic capacitance. On top of this disadvantage, the settling time of the S/H circuit during hold mode is longer for series sampling than for parallel sampling. The reason for this is because the value of V_{out} in series sampling is being reset to V_{CC} (or V_{DD}) for every sample, but this is not the case for parallel sampling.

Switched Op-Amp Based Sample-and-Hold Circuit:

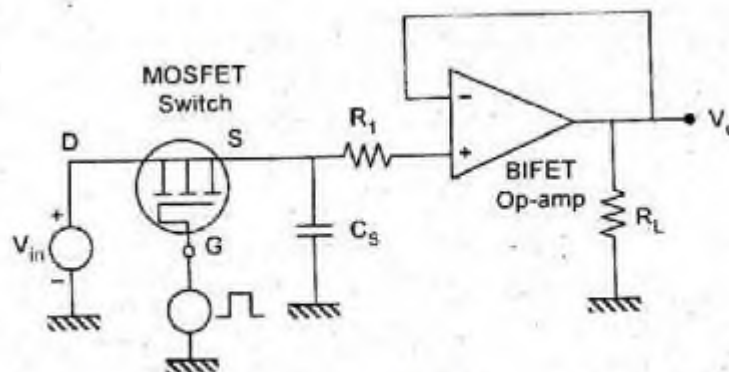
This S/H technique takes advantage of the fact that when a MOS transistor is in the saturation region, the channel is pinched off and disconnected from the drain. Therefore, if the hold capacitor is connected to the drain of the MOS transistor, charge injection will only go to the source junction, leaving the drain unaffected. Based on this concept, a switched op-amp (SOP) based S/H circuit, as shown in Figure



Switched op-amp based sample and hold circuit.

During sample mode, the SOP behaves just like a regular op-amp, in which the value of the output follows the value of the input. During hold mode, the MOS transistors at the output node of the SOP are turned off while they are still operating in saturation, thus preventing any channel charge from flowing into the output of the SOP. In addition, the SOP is shut off and its output is held at high impedance, allowing the charge on C_h to be preserved throughout the hold mode. On the other hand, the output buffer of this S/H circuit is always operational during sample and hold mode and is always providing the voltage on C_h to the output of the S/H circuit.

S/H circuits that operate in closed loop configuration can achieve high resolution, but their requirements for high gain circuit block, such as an op-amp, limits the speed of the circuits. As a result, better and faster S/H circuits must be developed.

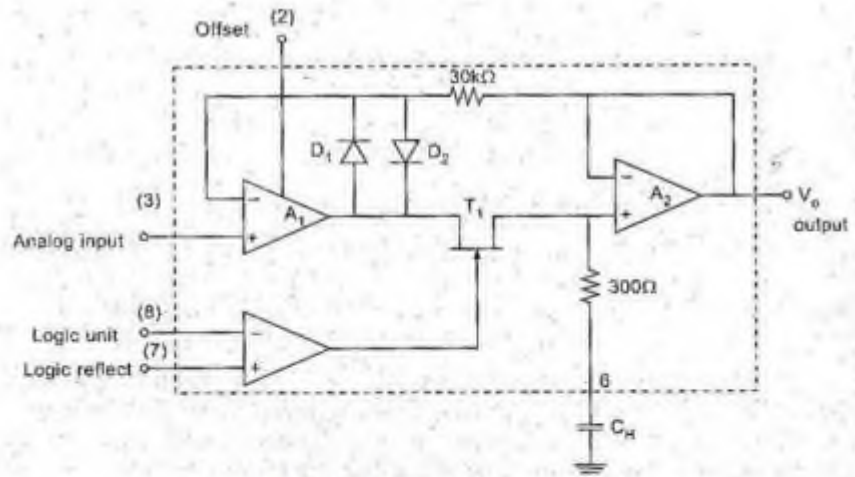


High speed Sample and Hold circuit with MOSFET

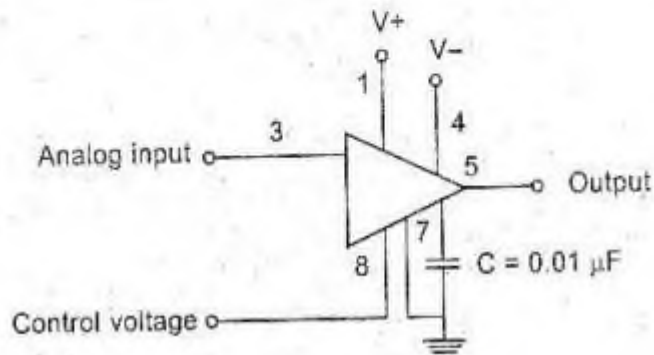
The above figure shows a sample and holds circuit with MOSFET as Switch acting as a sampling device and also consists of a holding capacitor C_s to store the sample values until the next sample comes in. This is a high speed circuit as it is apparent that CMOS switch has a very negligible propagation delay.

Three S/H circuits to reduce error:

- series sampling,
- SOP based S/H circuit,
- bottom plate S/H circuit with bootstrapped switch



LF 398 IC- Functional Diagram



Connections of S&H IC



Sigma-delta ADCs/ Over sampling Converters:

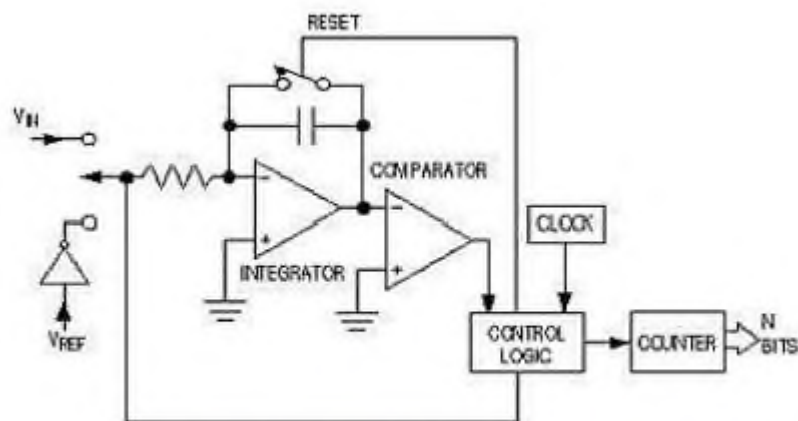
It consists of 2 main parts - modulator and digital filter. The modulator includes an integrator and a comparator with a feedback loop that contains a 1-bit DAC. The modulator oversamples the input signal, converting it to a serial bit stream with a frequency much higher than the required sampling rate. This is then transformed by the output filter to a sequence of parallel digital words at the sampling rate.

The characteristics of sigma-delta converters are

- high resolution
- high accuracy
- Low noise and low cost.
- Typical applications are for speech and audio.

A **Sigma-Delta ADC** (also known as a Delta-Sigma ADC) oversamples the desired signal by a large factor and filters the desired signal band. Generally, a smaller number of bits than required are converted using a Flash ADC after the Filter. The resulting signal, along with the error generated by the discrete levels of the Flash, is fed back and subtracted from the input to the filter. This negative feedback has the effect of noise shaping the error due to the Flash so that it does not appear in the desired signal frequencies.

A digital filter (decimation filter) follows the ADC which reduces the sampling rate, filters off unwanted noise signal and increases the resolution of the output. (sigma-delta modulation, also called delta-sigma modulation)



Sigma-delta ADCs/ Over sampling Converters: