EC 3352 – DIGITAL SYSTEM DESIGN

UNIT – III : SYNCHRONOUS SEQUENTIAL CIRCUITS

3.4 SYNCHRONOUS COUNTERS

Flip-Flops can be connected together to perform counting operations. Such a group of Flip- Flops is **counter**. The number of Flip-Flops used and the way in a which they are connected determine the number of states (called the modulus) and also the specific sequence of states that the counter goes through during each complete cycle.

Counters are classified into two broad categories according to the way they are clocked:

- Asynchronous counters, Synchronous counters.

In asynchronous (ripple) counters, the first Flip-Flop is clocked by the external clock pulse and then each successive Flip-Flop is clocked by the output of the preceding Flip-Flop.

In synchronous counters, the clock input is connected to all of the Flip-Flops so that they are clocked simultaneously. Within each of these two categories, counters are classified primarily by the type of sequence, the number of states, or the number of Flip-Flops in the counter.

The term ‘synchronous’ refers to events that have a fixed time relationship with each other. In synchronous counter, the clock pulses are

applied to all Flip- Flops simultaneously. Hence there is minimum propagation delay.

Table : 3.3 – Difference between Asynchronous and synchronous Counter

S.No	Asynchronous (ripple) counter	Synchronous counter
1	All the Flip-Flops are not clocked simultaneously.	All the Flip-Flops are clocked simultaneously.
2	The delay times of allFlip- Flops are added.Therefore there is considerable propagation delay.	There is minimum propagation delay.
3	Speed of operation is low	Speed of operation is high.
4	Logic circuit is very simple	Design involves complex logic circuit
	even for more number of states.	as number of state increases.
5	Minimum numbers of logic devices are needed.	The number of logic devices is more than ripple counters.
6	Cheaper than synchronous counters.	Costlier than ripple counters.

Bit Synchronous Binary Counter

In this counter the clock signal is connected in parallel to clock inputs of both the Flip-Flops (FF_0 and FF_1). The output of FF_0 is connected to J_1 and K_1 inputs of the second Flip-Flop (FF_1).

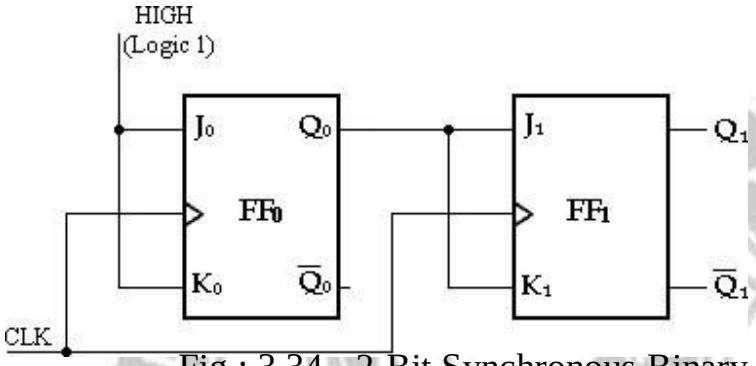

Fig : 3.34 - 2-Bit Synchronous Binary Counter

Assume that the counter is initially in the binary 0 state: i.e., both Flip-Flops are RESET. When the positive edge of the first clock pulse is applied, FF_0 will toggle because $J_0= k_0= 1$, whereas FF_1 output will remain 0 because $J_1= k_1= 0$. After the first clock pulse $Q_0=1$ and $Q_1=0$.

When the leading edge of CLK2 occurs, FF_0 will toggle and Q_0 will go LOW. Since FF_1 has a HIGH ($Q_0 = 1$) on its J_1 and K_1 inputs at the triggering edge of this clock pulse, the Flip-Flop toggles and Q_1 goes HIGH. Thus, after CLK2, $Q_0 = 0$ and $Q_1 = 1$.

When the leading edge of CLK3 occurs, FF_0 again toggles to the SET state ($Q_0 = 1$), and FF_1 remains SET ($Q_1 = 1$) because its J_1 and K_1 inputs are both LOW ($Q_0 = 0$).

After this triggering edge, $Q_0 = 1$ and $Q_1 = 1$.

Finally, at the leading edge of CLK4, Q_0 and Q_1 go LOW because they both have a toggle condition on their J_1 and K_1 inputs. The counter has now recycled to itsoriginal state, $Q_0 = Q_1 = 0$.

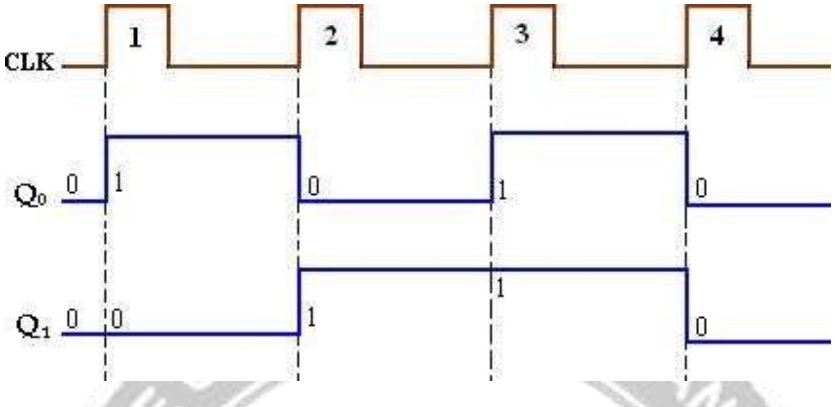

Fig : 3.35 - Timing diagram

3-Bit Synchronous Binary Counter

A 3 bit synchronous binary counter is constructed with three JK Flip-Flops andan AND gate. The output of FF_0 (Q_0) changes on each clock pulse as the counter progresses from its original state to its final state and then back to its original state. To produce this operation, FF_0 must be held in the toggle mode by constant HIGH, on its J_0 and K_0 inputs.

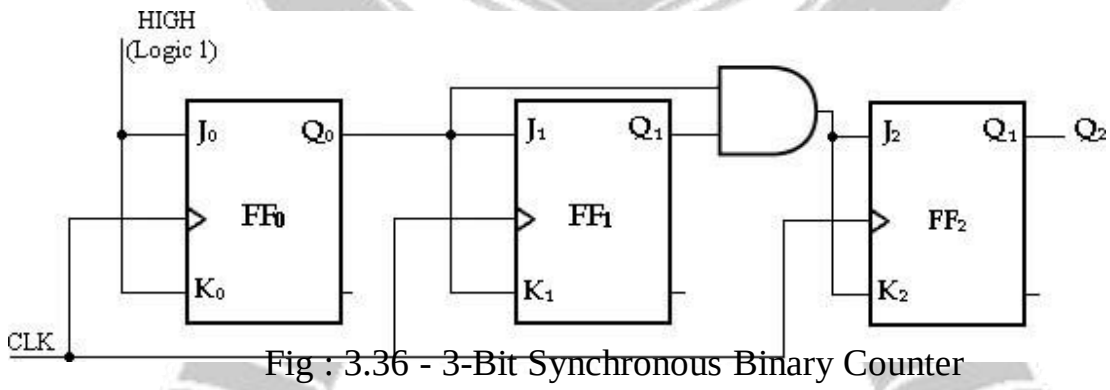

Fig : 3.36 - 3-Bit Synchronous Binary Counter

The output of FF_1 (Q_1) goes to the opposite state following each time Q_0= 1. This change occurs at CLK2, CLK4, CLK6, and CLK8. The CLK8 pulse causes the counter to recycle. To produce this operation, Q_0 is connected to the J_1 and K_1 inputs

of FF_1. When Q_0= 1 and a clock pulse occurs, FF_1 is in the toggle mode and therefore changes state. When Q_0= 0, FF_1 is in the no-change mode and remains in its present state.

The output of FF_2 (Q_2) changes state both times; it is preceded by the uniquecondition in which both Q_0 and Q_1 are HIGH. This condition is detected by the AND gate and applied to the J_2 and K_2 inputs of FF_3. Whenever both outputs Q_0= Q_1= 1, the output of the AND gate makes the J_2= K_2= 1 and FF_2 toggles on the following clock pulse. Otherwise, the J_2 and K_2 inputs of FF2 are held LOW by the AND gate output, FF_2 does not change state.

CLOCK Pulse	Q2	Q1	Q0
Initiall	0	0	0
y1	0	0	1
2	0	1	0
3	0	1	1
4	1	0	0
5	1	0	1
6	1	1	0
7	1	1	1
8 (recycles)	0	0	0

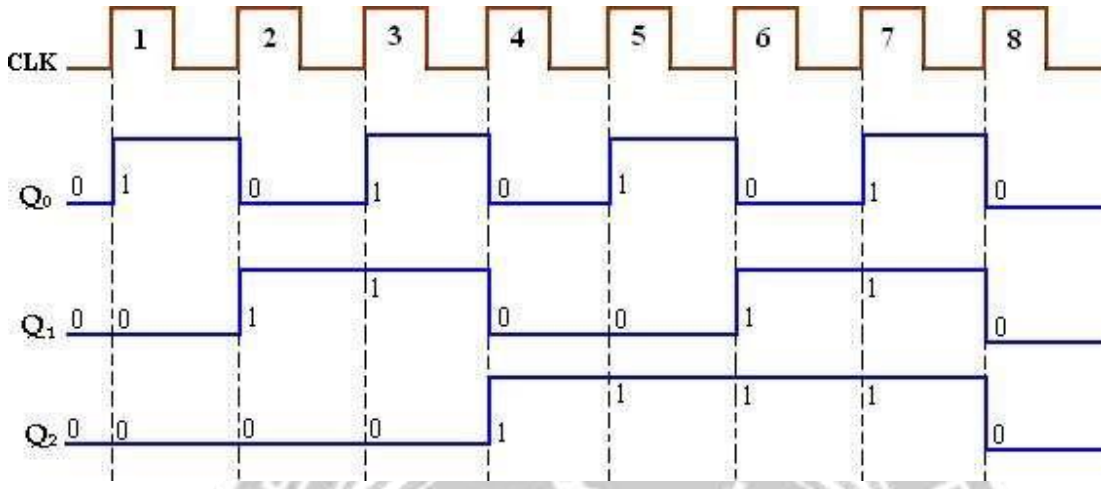

Fig : 3.37 - Timing diagram

4-Bit Synchronous Binary Counter

This particular counter is implemented with negative edge-triggered Flip-Flops. The reasoning behind the J and K input control for the first three Flip- Flops is the same as previously discussed for the 3-bit counter. For the fourth stage, the Flip- Flop has to change the state when $Q_0= Q_1= Q_2= 1$. This condition is decoded by AND gate G_3.

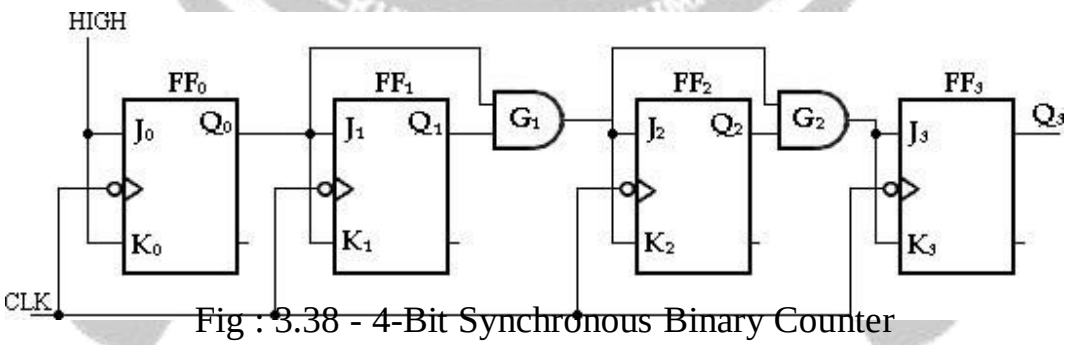

Fig : 3.38 - 4-Bit Synchronous Binary Counter

Therefore, when $Q_0= Q_1= Q_2= 1$, Flip-Flop FF_3 toggles and for all other times itis in a no-change condition. Points where the AND gate outputs are HIGH are indicated by the shaded areas.

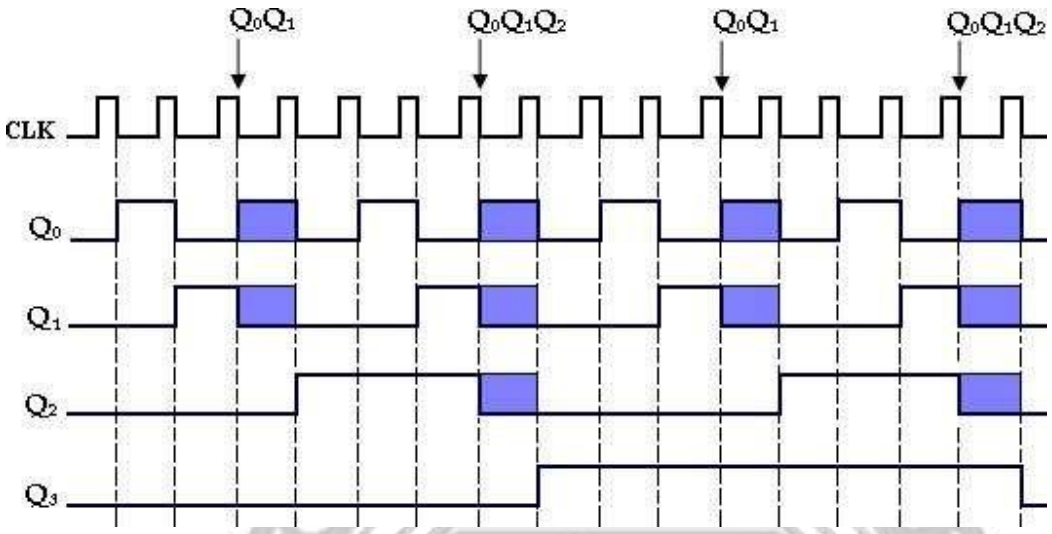

Fig : 3.39 - Timing diagram

4-Bit Synchronous Decade Counter: (BCD Counter):

BCD decade counter has a sequence from 0000 to 1001 (9). After 1001 state it must recycle back to 0000 state. This counter requires four Flip-Flops and AND/OR logic as shown below.

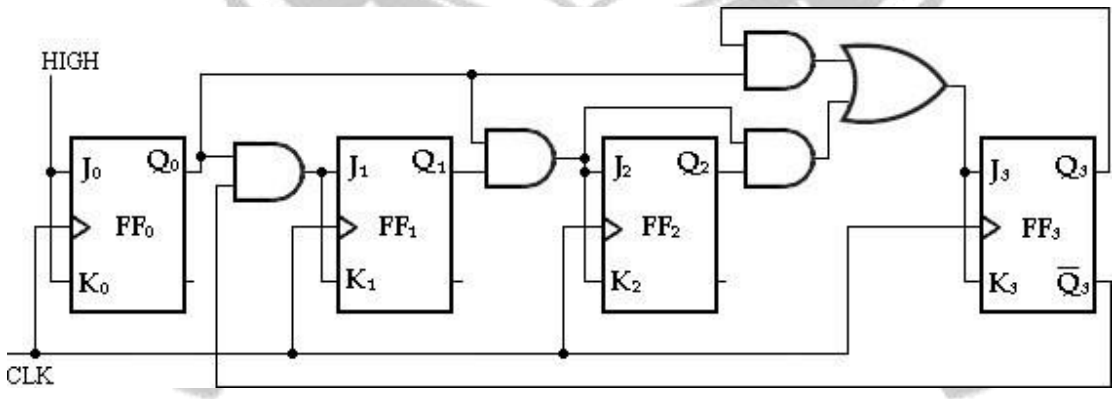

Fig : 3.39 - 4-Bit Synchronous Decade Counter

CLOCK Pulse	Q3	Q2	Q1	Q0
Initiall	0	0	0	0
y1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1
10(recycles)	0	0	0	0

xFirst, notice that FF_0 (Q_0) toggles on each clock pulse, so the logic equation for its J_0 and K_0 inputs is

$$\mathbf{J_0 = K_0 = 1}$$

This equation is implemented by connecting J_0 and K_0 to a constant HIGH level. xNext, notice from table, that FF_1 (Q_1) changes on the next clock pulse eachtime Q0 = 1 and Q3 = 0, so the logic equation for the J_1 and K_1 inputs is

$$\mathbf{J_1 = K_1 = Q_0 Q_3'}$$

This equation is implemented by ANDing Q_0 and Q_3 and connecting the gate outputto the J_1 and K_1 inputs of FF_l.

xFlip-Flop 2 (Q_2) changes on the next clock pulse each time both $Q_0 = Q_1 = 1$.

This requires an input logic equation as follows:

J2= K2= Q0Q1

This equation is implemented by ANDing Q_0 and Q_1 and connecting the gate outputto the J_2 and K_2 inputs of FF_3.

xFinally, FF_3 (Q_3) changes to the opposite state on the next clock pulse each time$Q_0 = 1$, $Q_1 = 1$, and $Q_2 = 1$ (state 7), or when $Q_0 = 1$ and $Q_1 = 1$ (state 9). The equation for this is as follows:

J3= K3= Q0Q1Q2+ Q0Q3

This function is implemented with the AND/OR logic connected to the J_3 and K_3 inputs of FF_3.

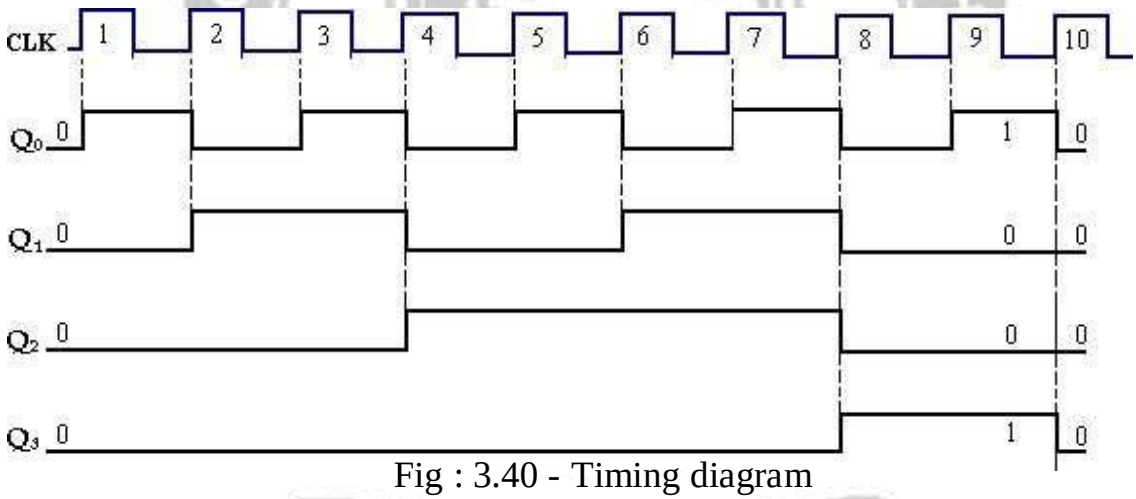

Fig : 3.40 - Timing diagram

Synchronous UP/DOWN Counter

An up/down counter is a bidirectional counter, capable of progressing in either direction through a certain sequence. A 3-bit binary counter that advances upward through its sequence (0, 1, 2, 3, 4, 5, 6, 7) and then can be reversed so

that it goes through the sequence in the opposite direction (7, 6, 5, 4, 3, 2, 1,0) is an illustration of up/down sequential operation.

The complete up/down sequence for a 3-bit binary counter is shown in table below. The arrows indicate the state-to-state movement of the counter for both its UP and its DOWN modes of operation. An examination of Q_0 for both the up and down sequences shows that FF_0 toggles on each clock pulse. Thus, the J_0 and K_0 inputs of

FF_0 are,

$J_0 = K_0 = 1$

CLOCK PULSE	UP	Q_2	Q_1	Q_0	DOWN
0		0	0	0	
1		0	0	1	
2		0	1	0	
3		0	1	1	
4		1	0	0	
5		1	0	1	
6		1	1	0	
7		1	1	1	

To form a synchronous UP/DOWN counter, the control input (UP/DOWN) is used to allow either the normal output or the inverted output of one Flip-Flop to the J and K inputs of the next Flip-Flop. When UP/DOWN= 1, the MOD 8 counter will count from 000 to 111 and UP/DOWN= 0, it will count from 111 to 000.

When UP/DOWN= 1, it will enable AND gates 1 and 3 and disable AND gates 2 and 4. This allows the Q0 and Q1 outputs through the AND gates to the J and K inputs of the following Flip-Flops, so the counter counts up as pulses are applied. When UP/DOWN= 0, the reverse action takes place.

$J_1 = K_1 = (Q_0.UP) + (Q_0'.DOWN)$

$J_2 = K_2 = (Q_0.\ Q_1.UP) + (Q_0'.Q_1'.DOWN)$

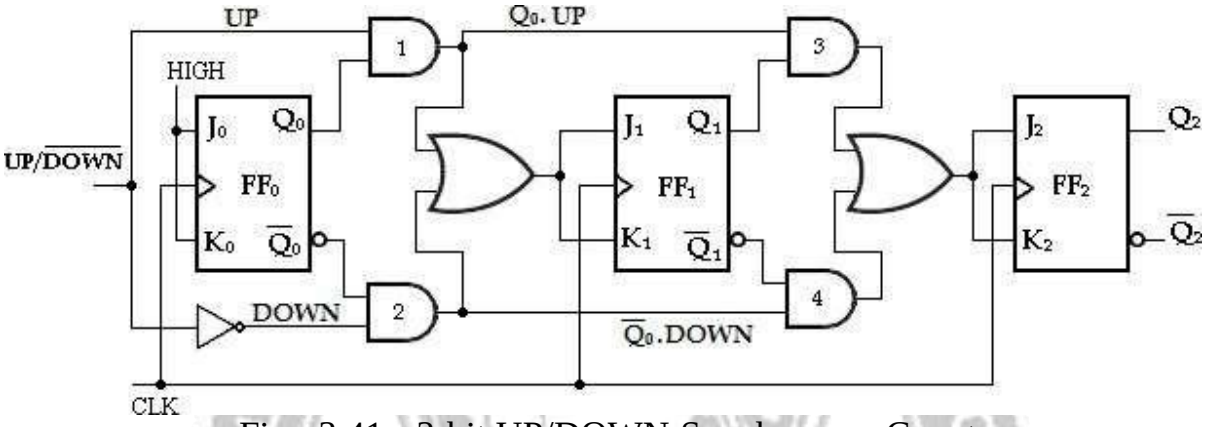

Fig : 3.41 - 3-bit UP/DOWN Synchronous Counter

MODULUS-N-COUNTERS

The counter with 'n' Flip-Flops has maximum MOD number 2^n. Find the number of Flip-Flops (n) required for the desired MOD number (N) using the equation,

$2n \geq N$

(i) For example, a 3 bit binary counter is a MOD 8 counter. The basic counter canbe modified to produce MOD numbers less than 2^n by allowing the counter to skin those are normally part of counting sequence.

n= 3 N= 8 2^n =

$2^3 = 8 = N$

(ii) MOD 5 Counter:

$2^n = N$

$2^n = 5$

2^2= 4 less than N.

2^3= 8 > N(5) Therefore, 3

Flip-Flops are required.

(iii) MOD 10 Counter:

2^n= N= 10 2^3= 8 less

than N.

2^4= 16 > N(10). To construct any MOD-N counter, the following methods can be used.

1. Find the number of Flip-Flops (n) required for the desired MOD number (N)using the equation,

   $2^n \geq N$.
2. Connect all the Flip-Flops as a required counter.
3. Find the binary number for N.
4. Connect all Flip-Flop outputs for which Q= 1 when the count is N, as inputs to NAND gate.
5. Connect the NAND gate output to the CLR input of each Flip-Flop.

When the counter reaches N^{th} state, the output of the NAND gate goes LOW, resetting all Flip-Flops to 0. Therefore the counter counts from 0 through N-1.

For example, MOD-10 counter reaches state 10 (1010). i.e., $Q_3Q_2Q_1Q_0$= 1 0 1 0. The outputs Q_3 and Q_1 are connected to the NAND gate and the output of the NAND gate goes LOW and resetting all Flip-Flops to zero. Therefore MOD-10 counter counts from 0000 to 1001. And then recycles to the zero value.

The MOD-10 counter circuit is shown below.

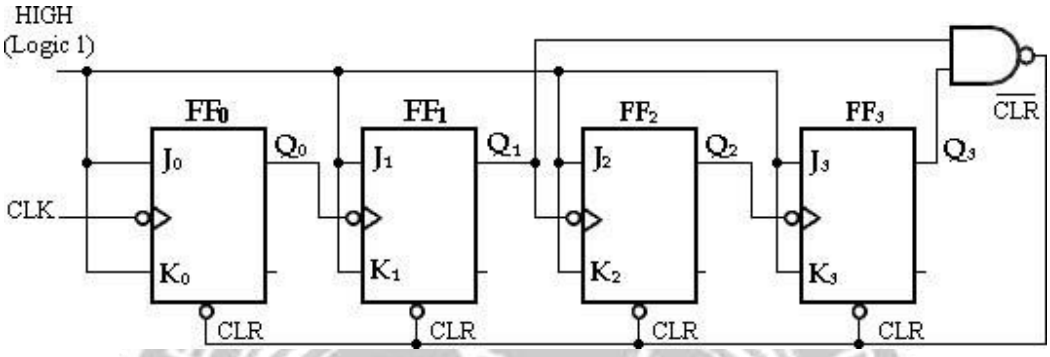

Fig : 3.42 - MOD-10 (Decade) Counter