### EC 3352 – DIGITAL SYSTEM DESIGN

#### <u>UNIT – IV : ASYNCHRONOUS SEOUENTIAL CIRCUITS</u>

# <u>4.1 Stable and Unstable states, output specifications Analysis transition</u> <u>table and flow table</u>

A sequential circuit is specified by a time sequence of inputs, outputs and internal states. In synchronous sequential circuits, the change of internal state occurs in response to the synchronized clock pulses. Asynchronous sequential circuits do not use clock pulses. The change of internal state occurs when there is a change in the input variables. The memory elements in synchronous sequential circuits are clocked flip- flops. The memory elements in asynchronous sequential circuits are either unclocked flip-flops or time -delay elements. The memory capability of a time-delay device depends on the finite amount of time it takes for the signal to propagate through digital gales. An asynchronous sequential circuit quite often resembles a combinational circuit with feedback.



Fig 4.1 - block diagram of an asynchronous sequential circuit

Image source from Digital Design by Moris Mano (Page No. 416)

The above figure shows the block diagram of an asynchronous sequential circuit that consists of a combinational circuit and delay elements connected to form feedback loops. There are n input variables, m output variables and k internal states. The delay elements can be visualized as providing short-term memory for the sequential circuit. In a gate-type circuit, the propagation delay that exists in the combinational circuit path from input to output provides sufficient delay along the feedback loop so that no specific delay elements are actually inserted into the feedback path. The present-state and next- state variables in asynchronous sequential circuits are customarily called secondary variables and excitation variables, respectively. The excitation variables should not be confused with the excitable table used in the design of clocked sequential circuits.

## ANALYSIS PROCEDURE

The analysis of asynchronous sequential circuits consists of obtaining a table or a diagram that describes the sequence of internal states and outputs as a function of changes in the Input variables. A logic diagram manifests the behavior of an asynchronous sequential circuit if it has one or more feedback loops or if it includes unclocked flip-flops.



Fig 4.2 – Example of an asynchronous sequential circuit EC 3352 – DIGITAL SYSTEM DESIGN

Image source from Digital Design by Moris Mano (Page No. 418) The diagram clearly shows two feedback loops from the OR gate outputs back to the AND gate inputs. The circuit consists of one input variable x and two internal states. The internal states have two excitation variab les,  $Y_1$ , and  $Y_2$  and two secondary variables, y1 and y2. The delay associated with each feedback loop is obtained from the propagation delay between eachY input and its corresponding youtput. Each logic gate in the path introduces a propagation delay of about 2 to 10 ns. The wires that conduct electrical signals introduce approximately a 1-ns delay for each foot of wire. Thus, no additional external delay elements are necessary when the combinational circuit and the wires in the feedback path provide sufficient delay.

The analysis of the circuit starts with a consideration of the excitation variables as outputs and the secondary variables as input s. We then derive the Boolean expressions for the excitation variables as a function of the input and secondary variables. These expressions readily obtained from the logic diagram are,

$$Y_1 = xy_1 + x'y_2$$
$$Y_2 = xy_1' + x'y_2$$

The next step is to plot the  $Y_1$  and  $Y_2$  functions in a map. The encoded binary values of the Y variables are used for labeling the rows and the input x variable is used to designate the columns.



Image source from Digital Design by Moris Mano (Page No. 418)

The transition table is obtained from the maps by combining the binary values in cores ponding square s, The transition table shows the value of  $Y = Y_1Y_2$  inside each square. The first bit of Y is obtained from the value of  $Y_1$  and the second bit is obtained from the value of  $Y_2$  in the same square position. For a stare to be stable, the secondary variables must match the excitation variables (i.e the value of Y must be the same as that of  $y = y_1y_2$ ). Those entries in the transition table where Y = y are circled to indicate stable condition. An un circled entry represents an unstable state.

The procedure for obtaining a transition table from the circuit diagrams of an asynchronous sequential circuit is as follows:

Determine all feedback loops in the circuit.

1. Designate the output of each feedback loop with variable Y; and its corresponding input with  $y_i$  for i = 1, 2, ..., k, where k is the number of feedback loops in the circuit.

2. Derive the Boolean functions of all Y's as a function of the external inputs and the y's 3.Plot each Y function in a map using the y variables for the rows and the

external inputs for the columns.

4. Combine all the maps into one table showing the value of  $Y = Y_1Y_2 \cdots Y_i$  inside eachsquare.

5. Circle those values of Y in each square that are equal to the value of  $y = y_1y_2...y_i$  in the same row.

### **FLOW TABLE**

During the design of asynchronous sequential circuits, it is more convenient to name the states by letter symbols without making specific reference to their binary values. Such a table is called a flow table and is similar to a transition table except that the internal states are symbolized with letters rather than binary numbers. The flow table also includes the output values of the circuit for each stable state.

GINEERIN



Image source from Digital Design by Moris Mano (Page No. 420)

If we assign the following binary values to the stares: a = 00, b = 01, c = 11 and d = 10. The table of Figure (a) is called a primitive now table because it has only one stable state in each row. Figure (b) shows a flow table with more than one stable table in the same row. It has two states a and b, two inputs  $x_1$  and  $x_2$  and one output z. The binary value of

the output variable is indicated inside the square next to the state symbol and is separated from the state symbol by a comma. From the flow table, we observe the following behavior of the circuit:  $Ifx_1 = 0$ , the circuit is in state a. If  $x_1$  goes to 1 while  $x_2$  is 0, the circuit goes to state b. With inputs  $x_1x_2 = 11$ , the circuit may be either in state a orin stale b. If it is in state a. the output is 0. and if it is in state b. the output is 1. State b is maintained if the inputs change from 10 to 11. The circuit stays in state a if the inputs change from 01 to 11. Remember that in fundamental mode two input variables cannot change simultaneously; therefore, we do not allow a change of inputs from 00 to 11.

In order to obtain the circuit described by a flow table, it is necessary to assign a distinct binary value to each state. Such an assignment converts the flow table into a transition table from which we can derive the logic diagram.



Fig 4.4 – Derivation of a circuit by flow table Image source from Digital Design by Moris Mano (Page No. 421)

EC 3352 - DIGITAL SYSTEM DESIGN