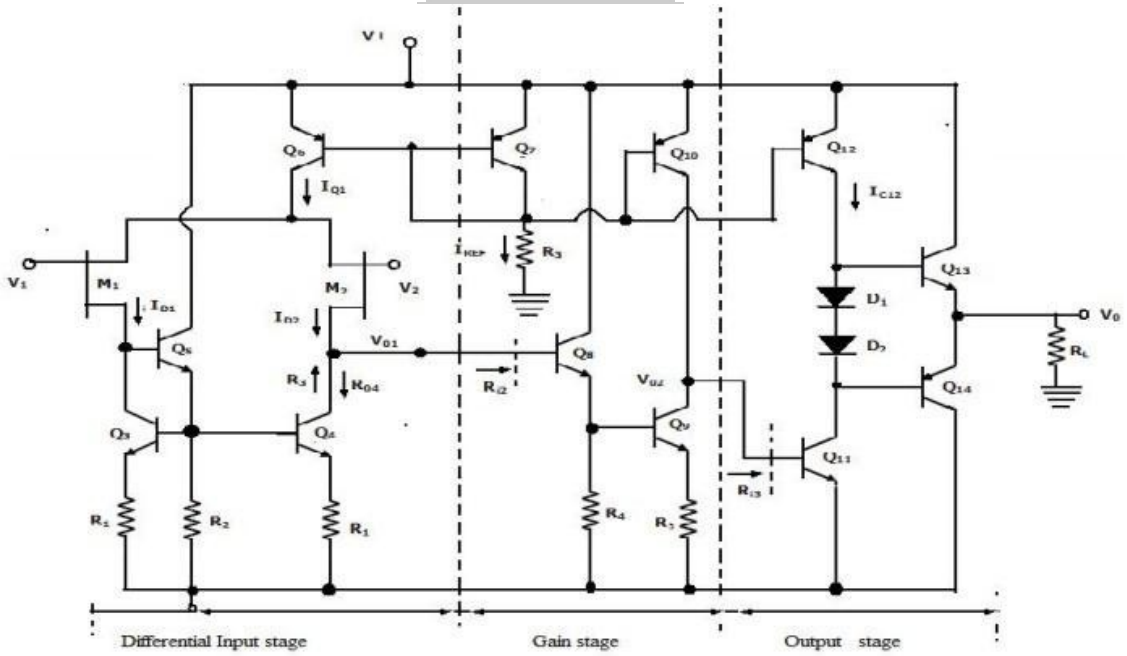
IC 741 Bipolar operational amplifier:

The IC 741 produced since 1966 by several manufactures is a widely used general purpose operational amplifier. Figure shows that equivalent circuit of the 741 op-amp, divided into various individual stages. The op-amp circuit consists of three stages.

1. The input differential amplifier
2. The gain stage
3. the output stage.

A bias circuit is used to establish the bias current for whole of the circuit in the I_C. The op-amp is supplied with positive and negative supply voltages of value ± 15V and the supply voltages as low as ±5V can also be used.



Bias Circuit:

The reference bias current IREF for the 741 circuit is established by the bias circuit consisting of two diodes-connected transistors Q_{11} and Q_{12} and resistor R_5. The Widlar current source formed by Q_{11}, Q_{10} and R_4 provide bias current for the differential amplifier stage at the collector of Q_{10}. Transistors Q_8 and Q_9 form another current mirror providing bias current for the differential amplifier. The reference bias current IREF also provides mirrored and proportional current at the collector of the double –collector lateral PNP transistor Q_{13}. The transistor Q_{13} and Q_{12} thus form a two-output current mirror with $Q_{13}A$ providing bias current for output stage and Q13B providing bias current for Q_{17}. The transistor Q_{18} and Q_{19} provide dc bias for the output stage. Formed by Q_{14} and Q_{20} and they establish two VBE drops of potential difference between the bases of Q_{14} and Q_{18}.

Input stage:

The input differential amplifier stage consists of transistors Q_1 through Q_7 with biasing provided by Q_8 through Q_{12}. The transistor Q_1 and Q_2 form emitter – followers contributing to high differential input resistance, and whose output currents are inputs to the common base amplifier using Q_3 and Q_4 which offers a large voltage gain. The transistors Q_5, Q_6 and Q_7 along with resistors R_1, R_2 and R_3 from the active load for input stage. The single-ended output is available at the collector of Q6. The two null terminals in the input stage facilitate the null adjustment. The lateral PNP transistors Q3 and Q4 provide additional protection against voltage breakdown conditions. The emitter-base junction Q3 and Q4 have higher emitter-base breakdown

voltages of about 50V. Therefore, placing PNP transistors in series with NPN transistors provide protection against accidental shorting of supply to the input terminals.

Gain Stage:

The Second or the gain stage consists of transistors Q_{16} and Q_{17}, with Q_{16} acting as an emitter – follower for achieving high input resistance. The transistor Q_{17} operates in common emitter configuration with its collector voltage applied as input to the output stage. Level shifting is done for this signal at this stage. Internal compensation through Miller compensation technique is achieved using the feedback capacitor C_1 connected between the output and input terminals of the gain stage.

Output stage:

The output stage is a class AB circuit consisting of complementary emitter follower transistor pair Q_{14} and Q_{20}. Hence, they provide an effective loss output resistance and current gain. The output of the gain stage is connected at the base of Q_{22}, which is connected as an emitter follower providing a very high input resistance, and it offers no appreciable loading effect on the gain stage. It is biased by transistor Q_{13}A which also drives Q18 and Q19, that are used for establishing a quiescent bias current in the output transistors Q_{14} and Q_{20}.