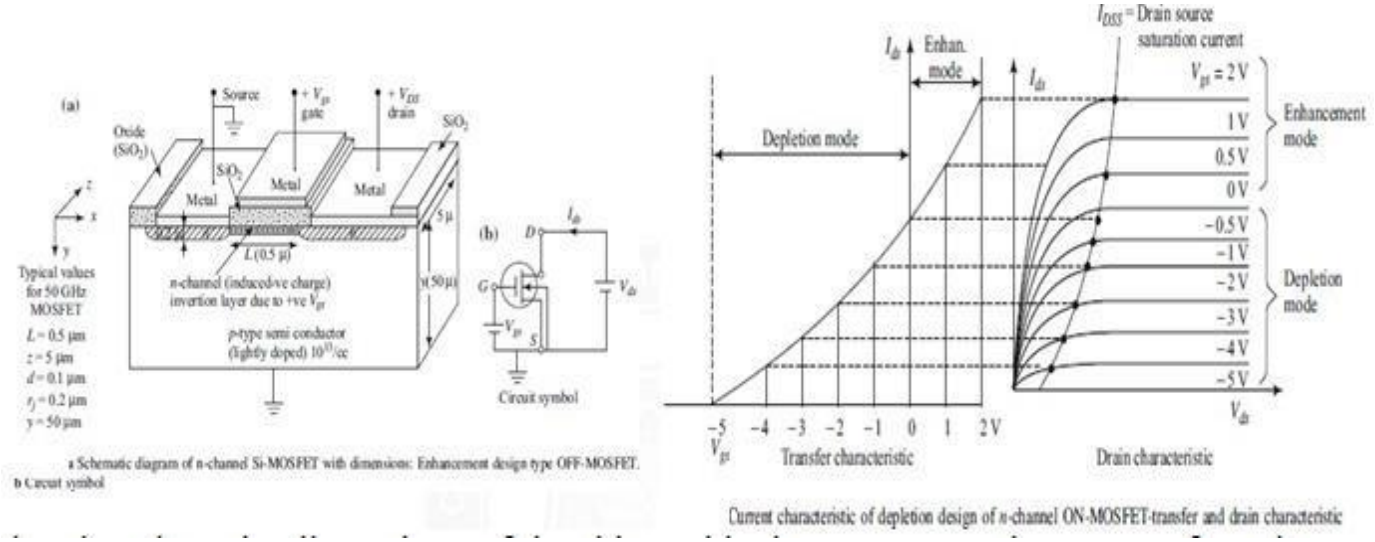
Power MOSFET

Power MOSFETs are well known for superior switching speed, and they require very little gate drive power because of the insulated gate. In these respects, power MOSFETs approach the characteristics of an "ideal switch". The main drawback is on-resistance RDS(on) and its strong positive temperature coefficient. This application note explains these and other main features of high voltage N-channel power MOSFETs, and provides useful information for device selection and application. All the transistors e.g. bipolar, Jn-FET, MESFET, are three terminal devices, with substrate isolated in Jn-FET and MESFET, while in bipolar transistor, the substrate is the collector itself bonded on the header directly. Thus MOSFET is a four-terminal device where substrate is 4th terminal normally connected to the source and is grounded. Rest of the three terminals being source, drain, and gate. In Jn-FET the p–n junction is at the gate while in MOSFET, there are two p–n junctions at source and drain itself. The MOSFET, because of its simpler structure and lower losses, has superseded the junction transistors (BJT and Jn-FET).

MOSFET is generally used as power amplifiers as they have some advantages over BJT, Jn-FET, and MESFET,

A power MOSFET is a specific type of metal–oxide–semiconductor field-effect transistor (MOSFET) designed to handle significant power levels. Compared to the other power semiconductor devices, such as an insulated-gate bipolar transistor (IGBT) or a thyristor, its main advantages are high switching speed and good efficiency at low voltages. It shares with the IGBT an isolated gate that makes it easy to drive. They can be subject to low gain, sometimes to a degree that the gate voltage needs to be higher than the voltage under control. The design of power MOSFETs was made possible by the evolution of MOSFET and CMOS technology, used for manufacturing integrated circuits since the 1960s. The power MOSFET shares its operating principle with its low-power counterpart, the lateral MOSFET. The power MOSFET, which is commonly used in power electronics, was adapted from the standard MOSFET and commercially introduced in the 1970s.

The power MOSFET is the most common power semiconductor device in the world, due



a Schematic diagram of n-channel Si-MOSFET with dimensions: Enhancement design type OFF-MOSFET.
b Circuit symbol

Current characteristic of depletion design of *n*-channel ON-MOSFET-transfer and drain characteristic

Fig: 1 Power MOSFET and Drain Characteristics

(Source: Electronic Circuit Analysis- K.LalKishore,)

to its low gate drive power, fast switching speed, easy advanced paralleling applied to the gate with respect to source, i.e. vgs, (with substrate and source grounded), then −ve charges are induced in the channel (like a capacitor) and this provides current flow in the channel. As this MOSFET (Fig.) is with p-substrate, the channel region forms −ve carrier channel for current flow and therefore called nchannel MOSFET. The structure given in Fig. also gives the dimensions of the chip and its layers. In practice on a wafer, a large number of such chips are fabricated and chips diced out of it. A MOSFET can be a partof a circuit on a chip also and in such cases the MOSFET is normally surrounded by a thick oxide to isolate it from the adjacent device in a microwave I.C. Two designs of MOSFET are used, e.g. enhancement design (OFF-MOSFET), where n-channel region being very lightly p–type doped (10^{13}/cc), it has very less carriers therefore even with Vds bias Id = 0 for Vg 0. But by Vg = +ve n carriers are induced in the channel region, then Id starts (Fig.): The other is depletion type depletion design(ON-MOSFET), where n type (10^{15}/cc) doping is already done in the channel region, giving enough n carriers. Therefore with Vds bias Id 6¼ 0, whether Vg 0 or Vg 0 and hence ON-type the name is given.

On-State Resistance:

When the power MOSFET is in the on-state (see MOSFET for a discussion on operation modes), it exhibits a resistive behaviour between the drain and source terminals. It can be seen in figure 2 that this resistance (called R_{DSon} for "drain to source resistance in on-state") is the sum of many elementary contributions:

- **R_S is the source resistance**. It represents all resistances between the source terminal of the package to the channel of the MOSFET: resistance of the wire bonds, of the source metallisation, and of the N^+ wells;
- **R_{ch}. This is the channel resistance**. It is inversely proportional to the channel width, and for a given die size, to the channel density. The channel resistance is one of the main contributors to the R_{DSon} of low-voltage MOSFETs, and intensive work has been carried out to reduce their cell size in order to increase the channel density;
- **R_a is the access resistance.** It represents the resistance of the epitaxial zone directly under the gate electrode, where the direction of the current changes from horizontal (in the channel) to vertical (to the drain contact);
- **R_{JFET} is the detrimental effect of the cell size reduction mentioned above**: the P implantations form the gates of a parasitic JFET transistor that tend to reduce the width of the current flow;
- **R_n is the resistance of the epitaxial layer**. As the role of this layer is to sustain the blocking voltage, R_n is directly related to the voltage rating of the device. A high voltage MOSFET requires a thick, low-doped layer, i.e., highly resistive, whereas a low-voltage transistor only requires a thin layer with a higher doping level, i.e., less resistive. As a result, R_n is the main factor responsible for the resistance of high-voltage MOSFETs;
- **R_D is the equivalent of R_S for the drain**. It represents the resistance of the transistor substrate (the cross section in figure 1 is not at scale, the bottom N^+ layer is actually the thickest) and of the package connections.

- **Switching Operation**

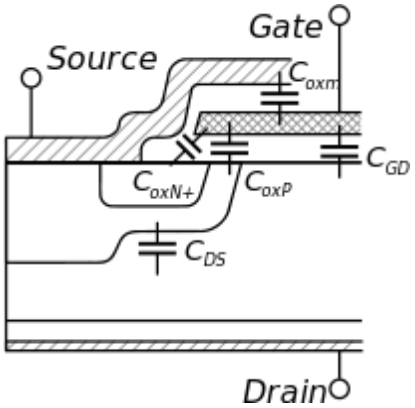


Fig:2 Switching Characteristics

(Source: Electronic Circuit Analysis- K.LalKishore)

- Because of their unipolar nature, the power MOSFET can switch at very high speed. Indeed, there is no need to remove minority carriers as with bipolar devices. The only intrinsic limitation in commutation speed is due to the internal capacitances of the MOSFET. These capacitances must be charged or discharged when the transistorswitches. This can be a relatively slow process because the current that flows through the gate capacitances is limited by the external driver circuit. This circuit will actually dictate the commutation speed of the transistor (assuming the power circuit has sufficiently low inductance).

Capacitances

In the MOSFET the capacitances are often named C_{iss} (input capacitance, drain and source terminal shorted), C_{oss} (output capacitance, gate and source shorted), and C_{rss} (reverse transfer capacitance, source connected to ground). The relationship between these capacitances and those described below is:

where C_{GS}, C_{GD} and C_{DS} are respectively the gate-to-source, gate-to-drain and drain-to-source capacitances (see below). Manufacturers prefer to quote C_{iss}, C_{oss} and C_{rss} because

they can be directly measured on the transistor. However, as C_{GS}, C_{GD} and C_{DS} are closer to the physical meaning, they will be used in the remaining of this article.

Gate to source capacitance

- The C_{GS} capacitance is constituted by the parallel connection of C_{oxN+}, C_{oxP} and C_{oxm} .As the N^+ and P regions are highly doped, the two former capacitances can be considered as constant. C_{oxm} is the capacitance between the (polysilicon) gate and the (metal) source electrode, so it is also constant. Therefore, it is common practice to consider C_{GS} as a constant capacitance, i.e. its value does not depend on the transistor state.

Gate to drain capacitance

The C_{GD} capacitance can be seen as the connection in series of two elementary capacitances. The first one is the oxide capacitance (C_{oxD}), constituted by the gate electrode, the silicon dioxide and the top of the N epitaxial layer. It has a constant value. The second capacitance (C_{GDj}) is caused by the extension of the space-charge zone when the MOSFET is in off-state. Therefore, it is dependent upon the drain to source voltage.

Packaging inductances

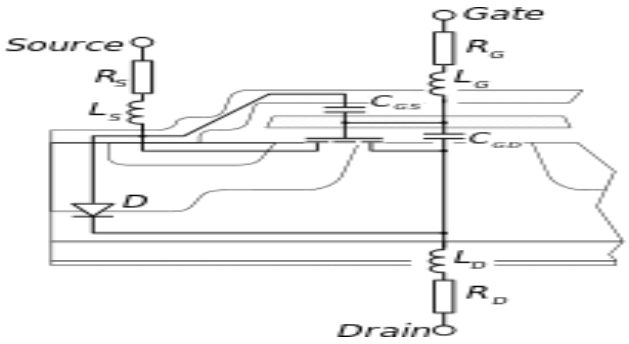


Fig: 3 **Packaging Inductances**

(Source: Electronic Circuit Analysis- K.LalKishore,)

To operate, the MOSFET must be connected to the external circuit, most of the time using wire bonding (although alternative techniques are investigated). These connections exhibit a parasitic inductance, which is in no way specific to the MOSFET technology, but has important effects because of the high commutation speeds. Parasitic inductances tend to maintain their current constant and generate overvoltage during the transistor turn off, resulting in increasing commutation losses.

A parasitic inductance can be associated with each terminal of the MOSFET. They have different effects:

- the gate inductance has little influence (assuming it is lower than some hundreds of nanohenries), because the current gradients on the gate are relatively slow. In some cases, however, the gate inductance and the input capacitance of the transistor can constitute an oscillator. This must be avoided, as it results in very high commutation losses (up to the destruction of the device). On a typical design, parasitic inductances are kept low enough to prevent this phenomenon;
- The drain inductance tends to reduce the drain voltage when the MOSFET turns on, so it reduces turn on losses. However, as it creates an overvoltage during turn-off, it increases turn-off losses;
- The source parasitic inductance has the same behaviour as the drain inductance, plusa feedback effect that makes commutation last longer, thus increasing commutation losses.

At the beginning of a fast turn-on, due to the source inductance, the voltage at the source (on the die) will be able to jump up as well as the gate voltage; the internal V_{GS} voltage will remain low for a longer time, therefore delaying turn-on.

At the beginning of a fast turn-off, as current through the source inductance decreases sharply, the resulting voltage across it goes negative (with respect to

the lead outside the package) raising the internal V_{GS} voltage, keeping the MOSFET on, and therefore delaying turn-off.

Gate Oxide Break down

The gate oxide is very thin (100 nm or less), so it can only sustain a limited voltage. In the datasheets, manufacturers often state a maximum gate to source voltage, around 20 V, and exceeding this limit can result in destruction of the component. Furthermore, a high gate to source voltage reduces significantly the lifetime of the MOSFET, with little to no advantage on R_{DSon} reduction.

To deal with this issue, a gate driver circuit is often used.

Maximum drain to source voltage

Power MOSFETs have a maximum specified drain to source voltage (when turned off), beyond which breakdown may occur. Exceeding the breakdown voltage causes the device to conduct, potentially damaging it and other circuit elements due to excessive power dissipation.

Maximum drain current

The drain current must generally stay below a certain specified value (maximum continuous drain current). It can reach higher values for very short durations of time (maximum pulsed drain current, sometimes specified for various pulse durations). The drain current is limited by heating due to resistive losses in internal components such as bond wires, and other phenomena such as electromigration in the metal layer.

Maximum temperature]

The junction temperature (T_J) of the MOSFET must stay under a specified maximum value

for the device to function reliably, determined by MOSFET die

- It can be seen that C_{GDj} (and thus C_{GD}) is a capacitance which value is dependent
- upon the gate to drain voltage. As this voltage increases, the capacitance decreases.

When the MOSFET is in on-state, C_{GDj} is shunted, so the gate to drain capacitance remains equal to C_{oxD}, a constant value.

- **Drain to source capacitance**

As the source metallization overlaps the P-wells (see figure 1), the drain and source terminals are separated by a P-N junction. Therefore, C_{DS} is the junction capacitance. This is a non-linear capacitance, and its value can be calculated using the same equation as for C_{GDj}. So far we have discussed the n-channel MOSFET only, but all these are true for pchannelMOSFET also, with n-replaced by p layout and packaging materials. The packaging often limits the maximum junction temperature, due to the molding compound and (where used) epoxy characteristics.

The maximum operating ambient temperature is determined by the power dissipation and thermal resistance. The junction-to-case thermal resistance is intrinsic to the device and package; the case-to-ambient thermal resistance is largely dependent on the board/mounting layout, heatsinking area and air/fluid flow.

The type of power dissipation, whether continuous or pulsed, affects the maximum operating temperature, due to thermal mass characteristics; in general, the lower the frequency of pulses for a given power dissipation, the higher maximum operating ambient temperature, due to allowing a longer interval for the device to cool down. Models, such as a Foster network, can be used to analyze temperature dynamics from power transients.

Safe operating area

The safe operating area defines the combined ranges of drain current and drain to source voltage the power MOSFET is able to handle without damage. It is represented graphically as an area in the plane defined by these two parameters. Both drain current and drain-to-source voltage must stay below their respective maximum values, but their product must also stay below the maximum power dissipation the device is able to handle. Thus, the device cannot be operated at its maximum current and maximum voltage simultaneously

Applications:

1. It can be linear power amplifier in the enhancement mode as C_{in} and g_m do not depend on Vg, while

   c_{out} is independent of v_{ds}.

2. Gate ac input signal can be quite large asn-channel depletion-type ON-MOSFET can operate fromdepletion-mode region (−Vg) to enhancement mode region (+Vg). Temperature Effect