## DECIMAL ADDER

## BCD (Binary coded decimal)Adder:

If two BCD digits are added then their sum result will not always be in BCD. Consider the two given examples.


In the first example, result is in BCD while in the second example it is not in BCD.
Four bits are needed to represent all $B C D$ digits $(0-9)$. But with four bits we can represent up to 16 values ( 0000 through 1111). The extra six values ( 1010 through 1111) are not valid BCD digits.

Whenever the sum result is ? 9 , it will not be in $B C D$ and will require correction to get a valid BCD result.

|  | Z3 Z2 Z1 Z0 | F |
| :---: | :---: | :---: |
|  | $\begin{array}{lllll}0 & 0 & 0 & 0\end{array}$ | 0 |
| * | $\begin{array}{llll}0 & 0 & 0 & 1\end{array}$ | 0 |
|  | $\begin{array}{lllll}0 & 0 & 1 & 0\end{array}$ | 0 |
|  | $\begin{array}{lllll}0 & 0 & 1 & 1\end{array}$ | 0 |
|  | $\begin{array}{lllll}0 & 1 & 0 & 0\end{array}$ | 0 |
|  | $\begin{array}{lllll}0 & 1 & 0 & 1\end{array}$ | 0 |
| (0)2.951 | $\begin{array}{llll}0 & 1 & 1 & 0\end{array}$ | 0 |
| -8-10 | $\begin{array}{llll} 0 & 1 & 1 & 1 \end{array}$ | 0 |
|  | 10000 | 0 |
|  | $\begin{array}{llll}1 & 0 & 0 & 1\end{array}$ | 0 |
|  | $\begin{array}{llll}1 & 0 & 1 & 0\end{array}$ | 1 |
|  | $\begin{array}{llll}1 & 0 & 1 & 1\end{array}$ | 1 |
|  | $1 \begin{array}{llll}1 & 1 & 0 & 0\end{array}$ | 1 |
|  | $\begin{array}{llll}1 & 1 & 0 & 1\end{array}$ | 1 |
|  | $\begin{array}{llll}1 & 1 & 1 & 0\end{array}$ | 1 |
|  | $1 \begin{array}{llll}1 & 1 & 1 & 1\end{array}$ | 1 |

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Correction is done through the addition of 6 to the result to skip the six invalid values as shown in the truth table by yellow color.

Consider the given examples of non-BCD sum result and its correction.


A BCD adder is a circuit that adds two BCD digits in parallel and produces a sum BCDdigit and a carry out bit.

The maximum sum result of a $B C D$ input adder can be 19. As maximum number in BCDis 9 and may be there will be a carry from previous stage also, so $9+9+1=19$

The following truth table shows all the possible sum results when two BCD digits areadded.

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| Dec | $\mathbf{C O}$ | $\mathrm{Z}_{3}$ | $\mathrm{Z}_{2}$ | $\mathrm{Z}_{1}$ | $\mathrm{Z}_{0}$ | F |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 1 | 0 | 0 | 0 | 0 | 1 | 0 |
| 2 | 0 | 0 | 0 | 1 | 0 | 0 |
| 3 | 0 | 0 | 0 | 1 | 1 | 0 |
| 4 | 0 | 0 | 1 | 0 | 0 | 0 |
| 5 | 0 | 0 | 1 | 0 | 1 | 0 |
| 6 | 0 | 0 | 1 | 1 | 0 | 0 |
| 7 | 0 | 0 | 1 | 1 | 1 | 0 |
| 8 | 0 | 1 | 0 | 0 | 0 | 0 |
| 9 | 0 | 1 | 0 | 0 | 1 | 0 |
| 10 | 0 | 1 | 0 | 1 | 0 | 1 |
| 11 | 0 | 1 | 0 | 1 | 1 | 1 |
| 12 | 0 | 1 | 1 | 0 | 0 | 1 |
| 13 | 0 | 1 | 1 | 0 | 1 | 1 |
| 14 | 0 | 1 | 1 | 1 | 0 | 1 |
| 15 | 0 | 1 | 1 | 1 | 1 | 1 |
| 16 | 1 | 0 | 0 | 0 | 0 | 1 |
| 17 | 1 | 0 | 0 | 0 | 1 | 1 |
| 18 | 1 | 0 | 0 | 1 | 0 | 1 |
| 19 | 1 | 0 | 0 | 1 | 1 | 1 |

The logic circuit that checks the necessary BCD correction can be derived by detecting the condition where the resulting binary sum is 01010 through 10011 (decimal 10through 19).

## OBSERVE OPTLALZ OUTSPREAD

The circuit of the BCD adder will be as shown in the figure.


$$
\begin{array}{cc}
\text { Carry } \\
\text { out }
\end{array} \quad \frac{\text { Carry }}{\text { in }}
$$



The two BCD digits, together with the input carry, are first added in the top 4-bit binary adder to produce the binary sum. The bottom 4-bit binary adder is used to add the correctionfactor to the binary result of the top binary adder.
$>$ When the Output carry is equal to zero, the correction factor equals zero.
$>$ When the Output carry is equal to one, the correction factor is 0110.
The output carry generated from the bottom binary adder is ignored, since it suppliesinformation already available at the output-carry terminal.

A decimal parallel adder that adds $\mathbf{n}$ decimal digits needs $\mathbf{n}$ BCD adder stages. The outputcarry from one stage must be connected to the input carry of the next higherorder stage.

