INTRODUCTION TO WAFER TO CHIP FABRICATION PROCESS FLOW

A wire segment can be described as two end points of an interconnect with no programmable switch between them. A sequence of one or more wire segments in an FPGA can be termed as a track. Typically an FPGA has logic blocks, interconnects and Input/Output blocks. Input Output blocks lie in the periphery of logic blocks and interconnect. Wire segments connect I/O blocks to wire segments through connection blocks. Connection blocks are connected to logic blocks, depending on the design requirement one logic block is connected to another and soon.

In Xilinx routing, connections are made from logic block into the channel through a connection block. As SRAM technology is used to implement Lookup Tables, connection sites are large. A logic block is surrounded by connection blocks on all four sides. They connect logic block pins to wire segments. Pass transistors are used to implement connection for output pins, while use of multiplexers for inputpins saves the number of SRAM cells required per pin. The logic block pins connecting to connection blocks can then be connected to any number of wire segments through switching blocks. In Xilinx routing, connections are made from logic block into the channel through a connection block. As SRAM technology is used to implement Lookup Tables, connection sites are large. A logic block is surrounded by connection blocks on all four sides. They connect logic block pins to wire segments. Pass transistors are used to implement connection for output pins, while use of multiplexers for inputpins saves the number of SRAM cells required per pin. The logic block pins connecting to connection blocks can then be connected to any number of wire segments through switching blocks. In Xilinx routing, connections are made from logic block into the channel through a connection block. As SRAM technology is used to

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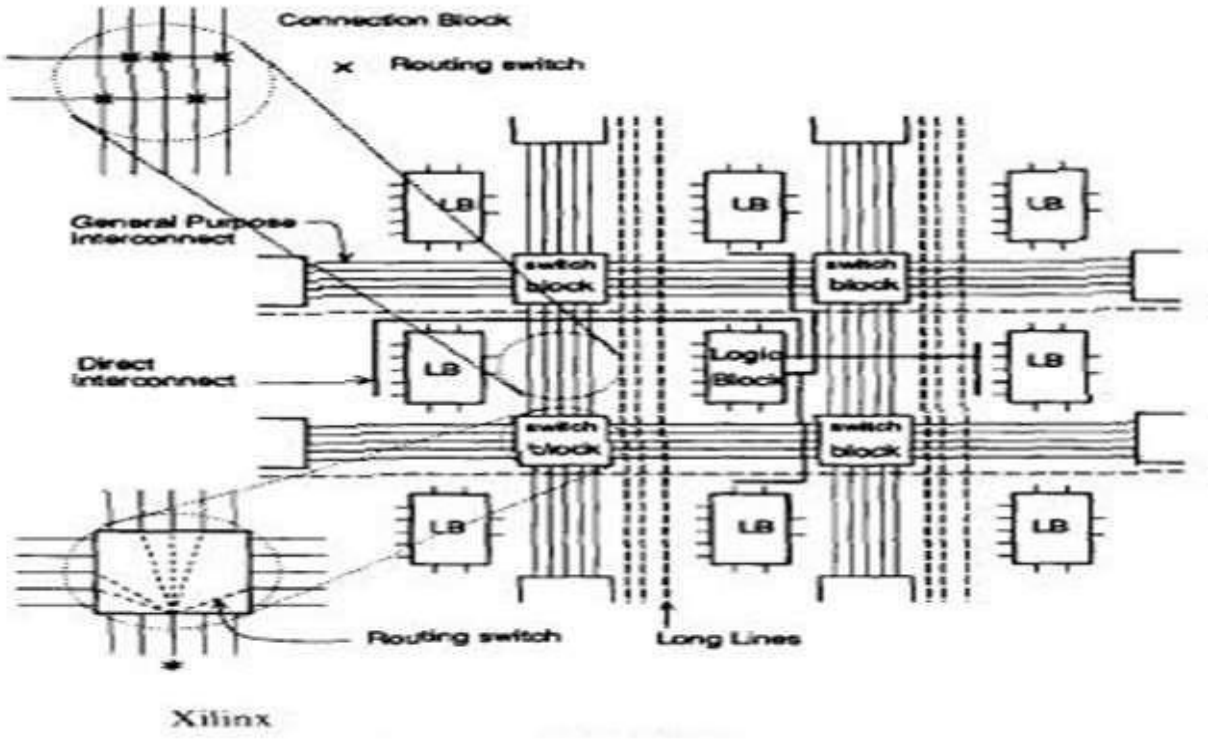

Fig 5.2.1: Routing Architecture

[Source: M.J. Smith, ―Application Specific Integrated Circuits]

There are four types of wire segments available :

- general purpose segments, the ones that pass through switches in the switchblock.
- Direct interconnect : ones which connect logic block pins to four

surroundingconnecting blocks

- long line : high fan out uniform delay connections
- clock lines : clock signal provider which runs all over the chip.

Fabrication process

Actel's design has more wire segments in horizontal direction than in vertical direction. The input pins connect to all tracks of the channel that is on the same side as the pin. The output pins extend across two channels above the logic block andtwo channels below it. Output pin can be connected to all 4 channels that it crosses. The switch blocks are distributed throughout the horizontal channels. All vertical tracks can make a connection with every incidental horizontal track. This allows for the flexibility that a horizontal track can switch into a vertical track, thus allowing

for horizontal and vertical routing of same wire. The drawback is more switches are required which add up to more capacitive load.

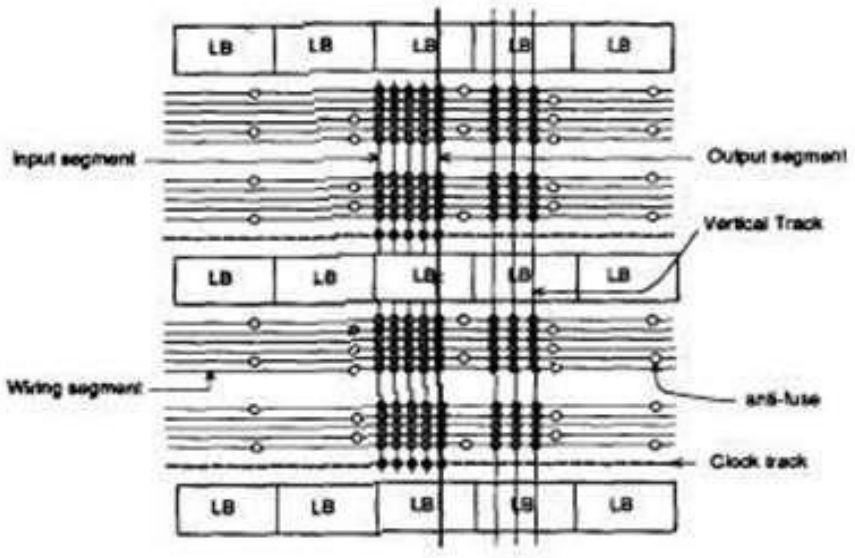

Fig 5.2.2: Actel FPGA Routing Architecture

[Source: M.J. Smith, —Application Specific Integrated Circuits]

Altera routing methodology

Altera routing architecture has two level hierarchy. At the first level of the hierarchy,16 or 32 of the logic blocks are grouped into a Logic Array Block, structure of the LAB is very similar to a traditional PLD. the connection is formed using EPROM- like floating-gate transistors. The channel here is set of wires that run vertically along the length of theFPGA.
Tracks are used for four types of connections :

- connections from output of all logic blocks in LAB.
- connection from logic expanders.
- connections from output of logic blocks in other LABs
- connections to and from Input output pads

All four types of tracks connect to every logic block in the array block. The connection block makes sure that every such track can connect to every logic block pin. Any track can connect to into any input which makes this routing simple. The intra-LAB routing consists of segmented channel, where segments are as long as possible. Global interconnect structure called programmable interconnect array(PIA) is used to make connections among LABs. Its internal structure is similarto internal routing of a LAB. Advantage of this scheme is that regularity of physicaldesign of silicon allows it to be packed tightly and efficiently. The disadvantage is the large number of switches required, which adds to capacitive load.