5.5 VHDL Behavioural Modelling Style

The behavioral modeling describes how the circuit should behave.

For these reasons, behavioral modeling is considered highest abstraction level as compared to data-flow or structural models.
The VHDL synthesizer tool decides the actual circuit implementation.

The VHDL behavioral model is widely used in test bench design, since the test bench design doesn't care about the hardware realization

Introduction to signal assignment

In VHDL-models, stimuli and responses occur through **signals**.

A signal can be declared only and exclusively in sections of concurrent code namely the architecture declaration section between the keyword **is** and **begin**.

A signal can be assigned:

to **ports**, which it is connected to

into **processes** which elaborates it

The simplest of these processes is the **signal assignment statement**.

Signal assignment statement

It will be shown that, according to the situation in which it is used, a signal assignment statement can be used in both concurrent and sequential code sections.

Its syntax is:

T <= S;

Meaning that the target signal T takes the value of source signal S.

This statement is executed whenever signal "T" change its value.

Signal "S" is in the sensitivity list of this statement.

VHDL Behavioral Modeling Style Example

In the structural modeling style page is reported the example of and_or entity structural architecture implementation. The following VHDL code implements the same functionality using a behavioral approach:

```
entity and_or is
port(
a : in std_logic;
b : in std_logic;
d : in std_logic;
e : in std_logic;
g : out std_logic);
```

```
end and_or;
architecture and_or_a of and_or is
-- declarative part: empty
begin
g <= (a and b) or (d and e);
end and_or_a;
```