2.2 BASIC CONFIGURATIONS, SYSTEM BUS TIMINGS, SYSTEM DESIGN USING 8086

BASIC CONFIGURATION

READ WRITE TIMING DIAGRAM - GENERAL BUS OPERATION

The 8086 has a combined address and data bus commonly referred as a time multiplexed address and data bus. The main reason behind multiplexing address and data over the same pins is the maximum utilization of processor pins and it facilitates the use of 40 pin standard DIP package. The bus can be demultiplexed using a few latches and transreceivers, whenever required.

Basically, all the processor bus cycles consist of at least four clock cycles. These are referredto as T1, T2, T3, T4. The address is transmitted by the processor during T1, It is present on the bus only for one cycle. The negative edge of this ALE pulse is used to separate the address and the data or status information as shown in Figure 2.2.1..

In maximum mode, the status lines S0, S1 and S2 are used to indicate the type of operation.Status bits S3 to S7 are multiplexed with higher order address bits and the BHE signal.

Address is valid during T1 while status bits S3 to S7 are valid during T2 through T4.

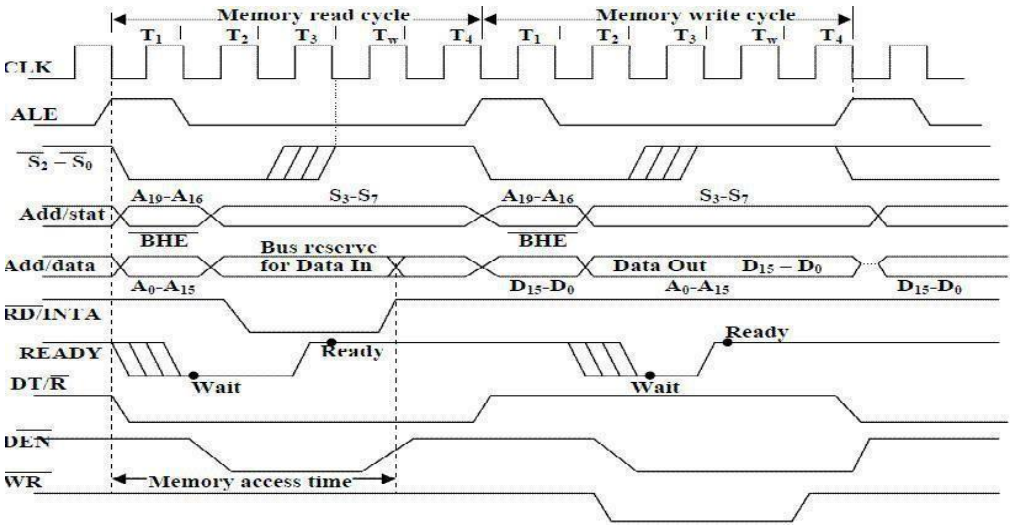

Figure 2.2.1. General Bus operation cycle

[Source: Advanced Microprocessors andMicrocontrollers by A.K Ray & K.M. Bhurchandi]

SYSTEM BUS TIMINGS:

MINIMUM MODE 8086 SYSTEM AND TIMINGS

In a minimum mode 8086 system, the microprocessor 8086 is operated in minimum mode by strapping its MN/MX* pin to logic1. In this mode, all the control signals are given out by the microprocessor chip itself. There is a single microprocessor in the minimum modesystem. The remaining components in the system are latches, transreceivers, clock generator,memory and I/O devices.

The opcode fetch and read cycles are similar. Hence the timing diagram can be categorized in two parts, the first is the timing diagram for read cycle and the second is the timing diagram for write cycle.

Figure 2.2.2 shows the read cycle timing diagram. The read cycle begins in T1 with the assertion of the address latch enable (ALE) signal and also M/IO* signal. During the negative going edge of this signal, the valid address is latched on the local bus. The BHE* and A0 signals address low, high or both bytes.

From Tl to T4, the M/IO* signal indicates a memory or I/O operation. At T2 the address is removed from the local bus and is sent to the output. The bus is then tristated. The read (RD*) control signal is also activated in T2 .The read (RD) signal causes the addressed device to enable its data bus drivers.

After RD* goes low, the valid data is available on the data bus. The addressed device will drive the READY line high, when the processor returns the read signal to high level, the addressed device will again tristate its bus drivers.

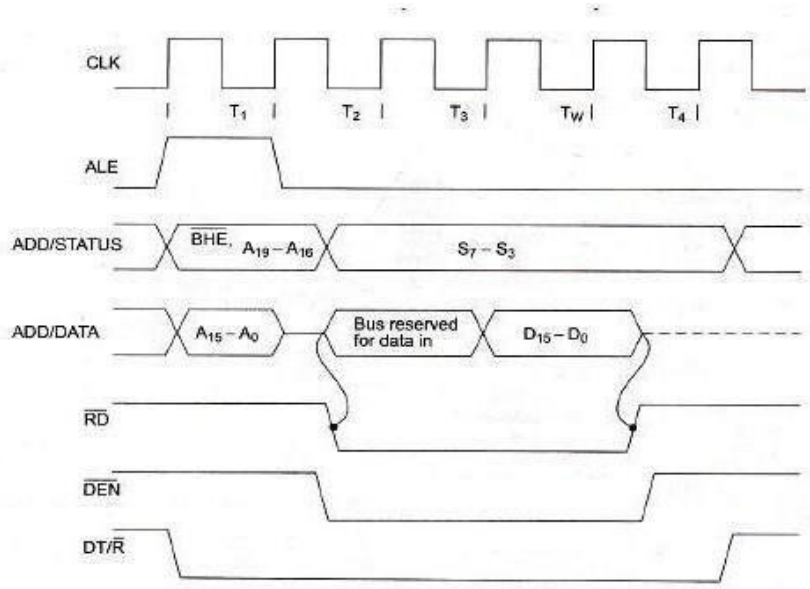

Figure 2.2.2 Read cycle timing diagram for minimum mode

[Source: AdvancedMicroprocessors and Microcontrollers by A.K Ray & K.M. Bhurchandi]

A write cycle also begins with the assertion of ALE and the emission of the address. The M/IO* signal is again asserted to indicate a memory or I/O operation. In T2 after sending theaddress in Tl the processor sends the data to be written to the addressed location. The data remains on the bus until middle of T4 state. The WR* becomes active at the beginning ofT2 (unlike RD* is somewhat delayed in T2 to provide time for floating). The BHE* and A0 signals are used to select the proper byte or bytes of memory or I/O word to be read or written. The M/IO*, RD* and WR* signals indicate the types of data transfer .

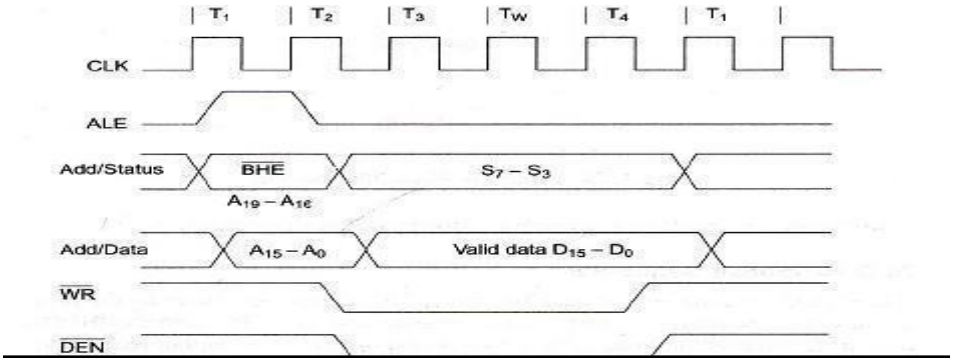

Figure 2.2.3 Write cycle timing diagram for minimum mode

[Source: AdvancedMicroprocessors and Microcontrollers by A.K Ray & K.M. Bhurchandi]

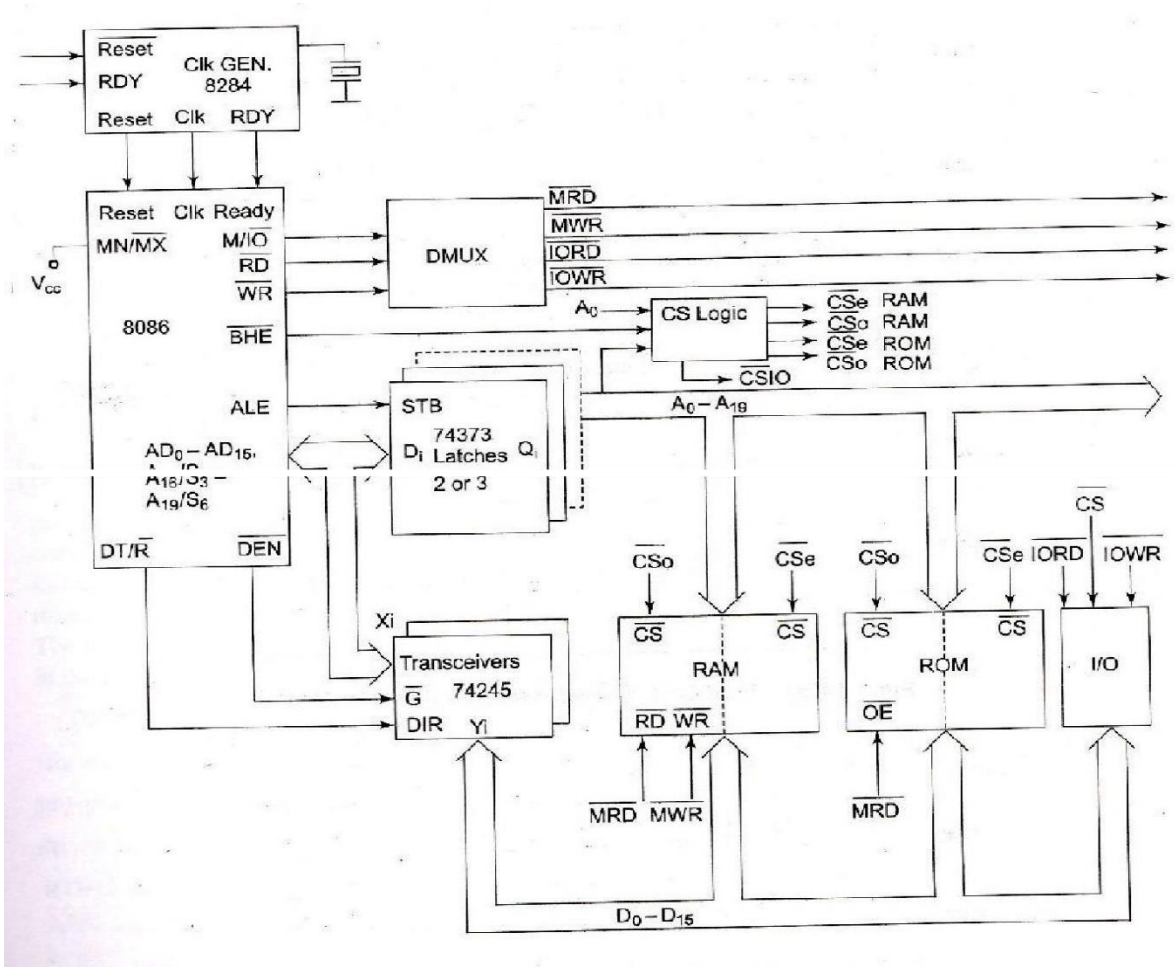

Figure 2.2.4 Minimum mode configuiration

[Source: Advanced Microprocessors andMicrocontrollers by A.K Ray & K.M. Bhurchandi]

SYSTEM DESIGN USING 8086

MAXIMUM MODE 8086 SYSTEM AND TIMINGS

In the maximum mode, the 8086 is operated by strapping the MN/MX* pin to ground. In thismode, the processor derives the status signals S2*, S1* and S0*. Another chip called bus controller derives the control signals using this status information. In the maximum mode, there may be more than one microprocessor in the system configuration.

The basic functions of the bus controller chip IC8288, is to derive control signals likeRD* and WR* (for memory and I/O devices), DEN*, DT/R*, ALE, etc. using the information made available by the processor on the status lines. The bus controller chip has input lines S2*, S1* and S0* and CLK. The CPU drives these inputs to 8288. It derives the outputs ALE, DEN*, DT/R*, MWTC*, AMWC*, IORC*, IOWC* and AIOWC*. The AEN*, IOB and CEN pins are especially useful for multiprocessor systems. AEN* and IOB are generally grounded. CEN pin is usually tied to+5V.

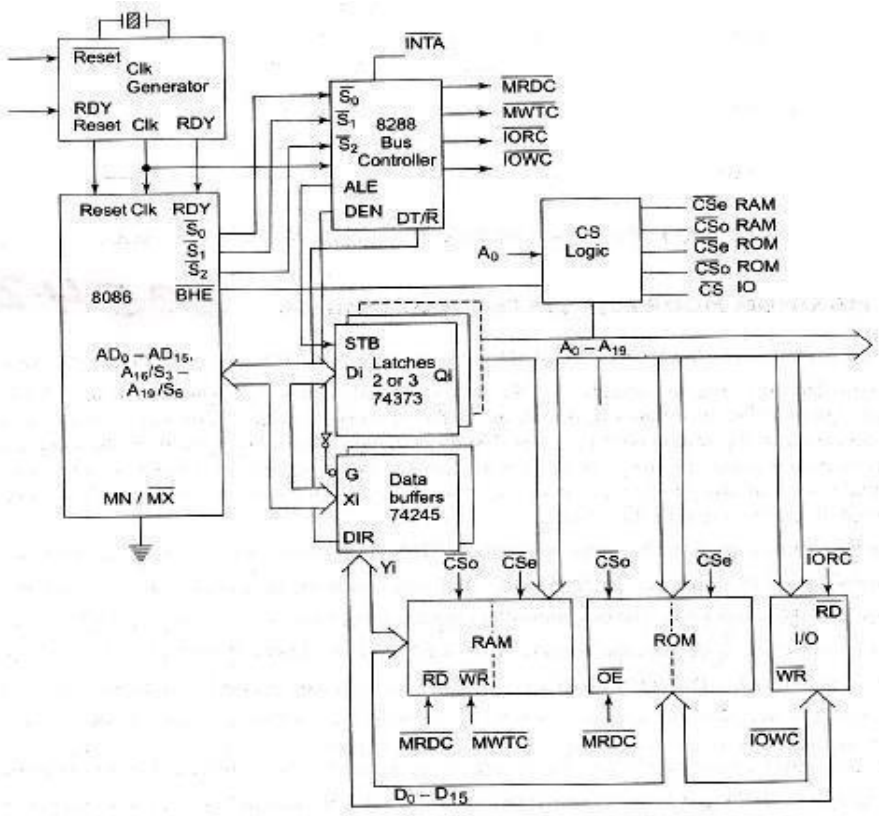

Figure 2.2.5 Maximum mode configuiration

[Source: Advanced Microprocessors andMicrocontrollers by A.K Ray & K.M. Bhurchandi]

The significance of the MCE/PDEN* output depends upon the status of the IOB pin. If IOB is grounded, it acts as master cascade enable to control cascaded 8259A; else it acts as peripheral data enable used in the multiple bus configurations.

INTA* pin is used to issue two interrupt acknowledge pulses to the interrupt controller or to an interrupting device.

IORC*, IOWC* are I/O read command and I/O write command signals respectively.

These signals enable an IO interface to read or write the data from or to the addressed port. The MRDC*, MWTC* are memory read command and memory write command signals respectively and may be used as memory read and write signals. All these command signals instruct the memory to accept or send data from or to the bus.

For both of these write command signals, the advanced signals namely AIOWC* and AMWTC* are available. They also serve the same purpose, but are activated one clock cycle earlier than the IOWC* and MWTC* signals, respectively. The maximum mode system is shown in Figure 2.2.5.

The maximum mode system timing diagrams are also divided in two portions as read (input) and write (output) timing diagrams. The address/data and address/status timings are similar to the minimum mode. ALE is asserted in T1, just like minimum mode. The only difference lies in the status signals used and the available control and advanced command signals. The Figure 2.2.6 shows the maximum mode timings for the read operation while the Figure 2.2.7 shows the same for the write operation.

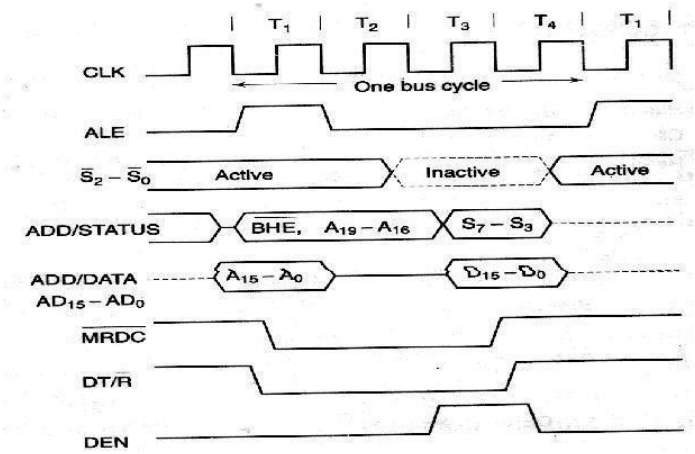

Figure 2.2.6 Memory Read Cycle

[Source: Advanced Microprocessors and Microcontrollers by A.K Ray & K.M. Bhurchandi]

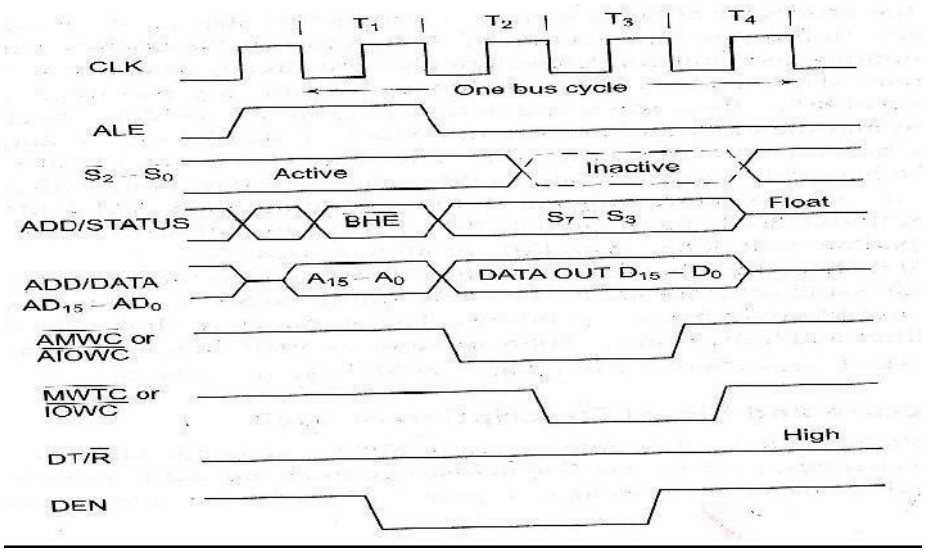

Figure 2.2.7 Memory write cycle

[Source: Advanced Microprocessors andMicrocontrollers by A.K Ray & K.M. Bhurchandi]

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