MPSoC's and Shared Memory Multiprocessors

Single processors may be sufficient for low-performance applications that are typical of early microcontrollers, but an increasing number of applications require multiprocessors to meet their performance goals.

Multiprocessor Systems-on-Chips (MPSoC) are one of the key applications of today. MPSoC are increasingly used to build complex integrated system. A MPSoC is more than just a rack of processors shrunk down to a single chip.

Definition : Multiprocessor is parallel processors with a single shared address.

Microprocessor is now the most cost-effective processor. Multiprocessors have the highest absolute performance-faster than the fastest uniprocessor.

Parallel processing program is a single program that runs on multiple processors simultaneously.

Cluster is a set of computers connected over a Local Area Network (LAN) that function as a single large multiprocessor.

Shared memory is a memory for a parallel processor with a single address space, implying implicit communication with loads and stores.

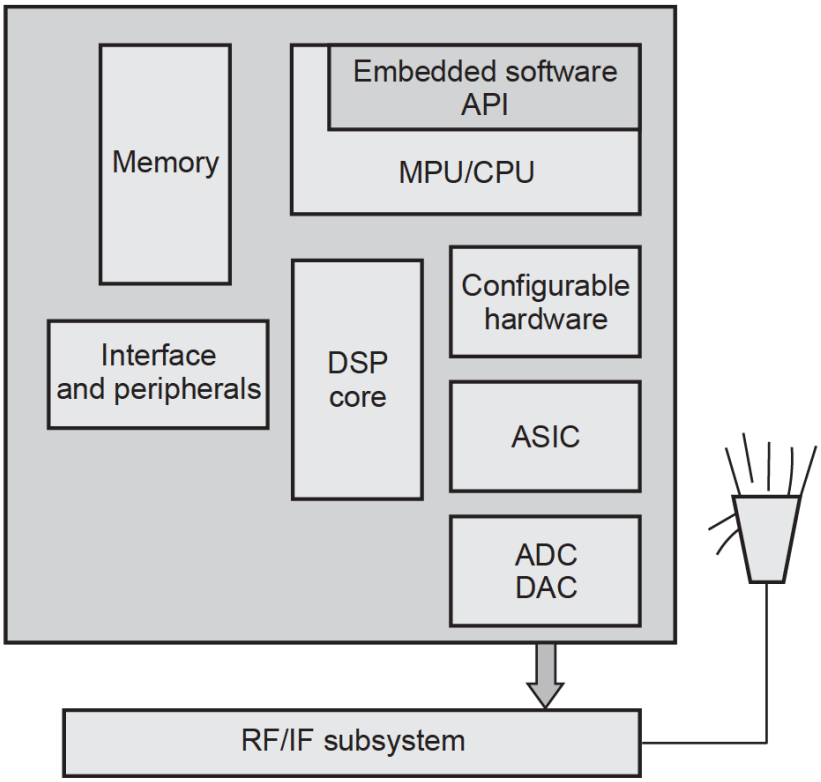
The typical MPSoC is a heterogeneous multiprocessor : there may be several different types of PEs, the memory system may be heterogeneously distributed around the machine, and the interconnection network between the PEs and the memory may also be heterogeneous

MPSoCs often require large amounts of memory. The device may have embedded memory on-chip as well as relying on off-chip commodity memory.

System-on-Chip (SoC) designs increasingly become the driving force of a number of modem electronics systems. Conceptually System on Chip refers to integrating the components of a board onto a single chip. Looks straightforward but productivity levels are too low to make it a reality.

The SoC chip includes : Embedded processor, ASIC logics and analog circuitry and Embedded memory.

The SoC software includes : OS, compiler, simulator, firmware, driver, protocol stack Integrated development environment (debugger, linker, ICE) application interface (C/C++, assembly).

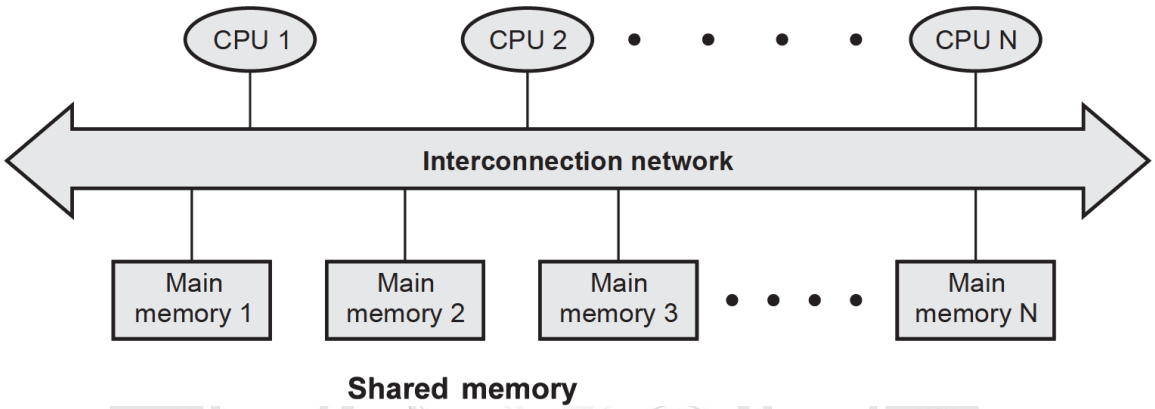


System on chip

1. Memory controller : Interfaces with the onboard RAM.
2. DMA : Handles the automated transfers of data between the RAM and memory-mapped hardware.
3. USB controller : Manages the hardware side of the device's USB connections.
4. DSP core : It provides hardware acceleration for some signal processing, such as JPEG encoding.
5. Display : Enables the SoC to drive various display types.
6. Camera : Allows the SoC to interface with a camera.

7. Storage : Manages I/O with the various types of storage that can be used with the SoC.
8. Debug : Enables the SoC to be connected to hardware debugging tools through various mechanisms, such as JTAG.

It consists of a pool of processors and a pool of memory are connected by an interconnection network.



A shared-memory model is often preferred because it makes life simpler for the programmer. The Raw architecture is a recent example of a regular architecture designed for high-performance computation

Signal address : Offer the programmer a single memory address space that all processors share. Processors communicate through shared variables in memory, with all processors capable of accessing any memory location via loads and stores.

Message passing : Communicating between multiple processors by explicitly sending and receiving information.

Heterogeneous memory systems : Some blocks of memory may be accessible by only one or a few processors. Heterogenous memory systems are harder to program because the programmer must keep in mind what processors can access what memory blocks

Irregular memory structures are often necessary in MPSoCs. One reason that designers resort to specialized memory is to support real-time performance.

Challenges and Opportunities

MPSoCs combine the difficulties of building complex hardware systems and complex software systems.

Methodology is critical to MPSoC design. Methodologies that work offer many advantages. They decrease the time it takes to design a system; they also make it easier to predict how long the design will take and how many resources it will require. Methodology also modify techniques for improving performance and power consumption that developers can apply to many different designs.

Methodology will necessarily be a moving target for the next decade.

MPSoC hardware architectures present challenges in all aspects of the multiprocessor : processing elements, memory and interconnects.

Configurable processors with customized instruction sets are one way to improve the characteristics of processing elements; hardware/software code sign of accelerators is another technique.