2.9 MULTI EMITTER TRANSISTOR

When the input is HIGH, the emitter base junction of Q1 is reverse-biased and current flows through R, base collector junction of Q1, is forward-biased into the base of Q2. Thus, the collector of transistor Q1 operates as an emitter and the emitter as a collector and the transistor Q2 is pulled into saturation resulting in a LOW output. When the input is LOW, the emitter-base junction of Q1 is forward-biased. The charge stored in the base of flows through the collector of transistor Q1.

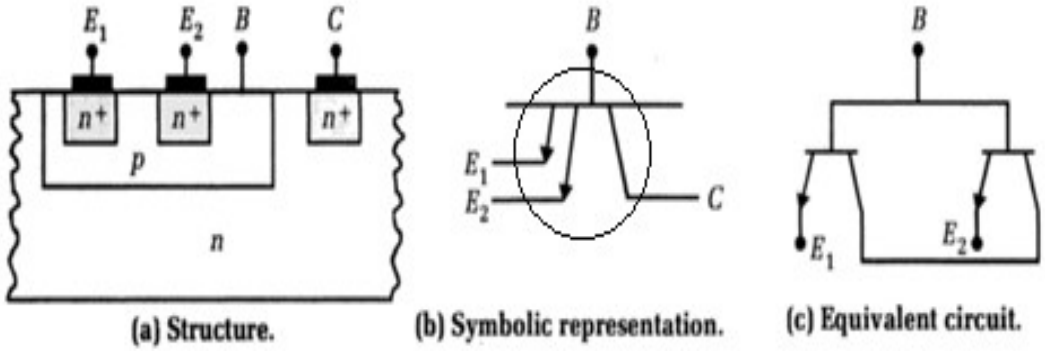

Fig:2.9.1 Multi Emitter Transistor

(Source : Linear Integrated Circuits)

When the input is HIGH, Q2 is in saturation with a base-to-ground voltage = 0.75V, indicating that the base-emitter junction of Q1 is reverse-biased. The transistor operates with an inverse common-base current gain α_I. Since it operates in the inversion region, the corresponding common-collector current gain is

$$h_{FC} = \frac{\alpha_I}{1-\alpha_I}$$

Designing low value of current gain minimizes the loading effect on the driving source when the input is HIGH. In order to achieve this,