3.6 KEYBOARD DISPLAY CONTROLLER

8279 - PROGRAMMABLE KEYBOARD CONTROLLER

8279 programmable keyboard/display controller is designed by Intel that interfaces a keyboard with the CPU. The important features of 8279 are

- Simultaneous keyboard and display operations
- Scanned keyboard mode
- Scanned sensor mode
- 8-character keyboard FIFO
- 16-character display
- Right or left entry
- 16-byte display RAM.
- Programmable scan timing

The keyboard first scans the keyboard and identifies if any key has been pressed. It then sends their relative response of the pressed key to the CPU and vice-a-versa.

The Keyboard can be interfaced either in the interrupt or the polled mode.
In the **Interrupt mode**, the processor is requested service only if any key is pressed, otherwise the CPUwill continue with its main task.

In the **Polled mode**, the CPU periodically reads an internal flag of 8279 to check whether any key ispressed or not with key pressure.

BLOCK DIAGRAM OF 8279:

The functional block diagram of 8279 is shown in Figure 3.6.1.

The four major sections of 8279 are keyboard, scan, display and CPU interface.

Keyboard section:

The keyboard section consists of eight return lines RL0 – RL7 that can be used to form the columns of a keyboard matrix. It has two additional input : shift and control/strobe. The keys are automatically debounced.

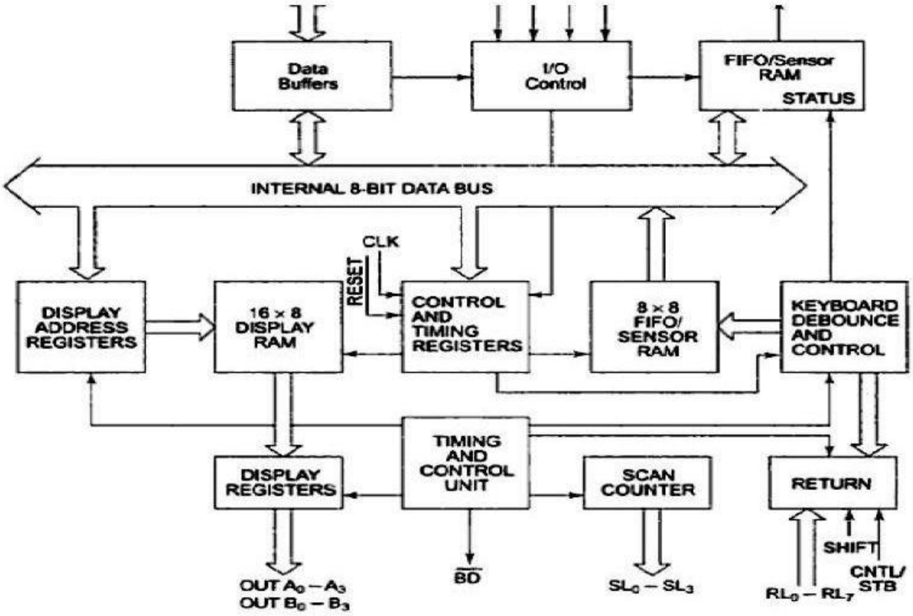


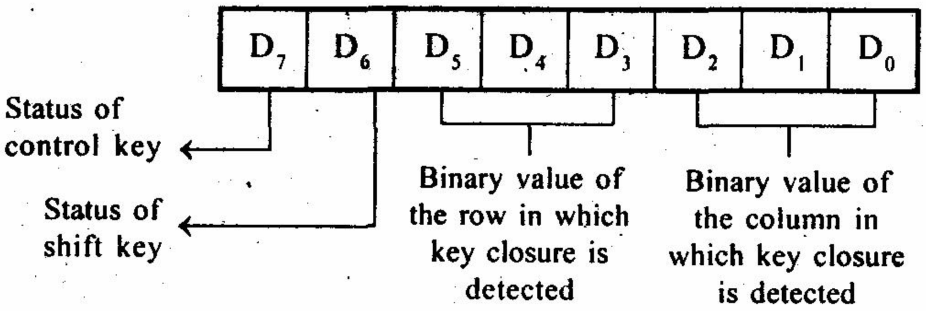
Figure 3.6.1 Internal blocks of Keyboard display controller

[Source: Advanced Microprocessors and Microcontrollers by A.K Ray & K.M.Bhurchandi]

The two operating modes of keyboard section are 2-key lockout and N-key rollover. In the 2-key lockout mode, if two keys are pressed simultaneously, only the first key is recognized. In the N-key rollover mode simultaneous keys are recognized and their codes are stored in FIFO.

The keyboard section also has an 8 x 8 FIFO (First In First Out) RAM. The FIFO can store eight key codes in the scan keyboard mode. The status of the shift key and control key are also stored along with key code. The 8279 generate an interrupt signal when there is an entry in FIFO.

The format of key code entry in FIFO for scan keyboard mode is,



In sensor matrix mode the condition (i.e., open/close status) of 64 switches is stored in FIFO RAM. If the condition of any of the switches changes then the 8279 asserts IRQ as high to interrupt the processor.

DISPLAY SECTION:

The display section has eight output lines divided into two groups A0-A3 and B0-B3. The output lines can be used either as a single group of eight lines or as two groups of four lines, in conjunction with the scan lines for a multiplexed display. The output lines are connected to the anodes through driver transistor in case of common cathode 7-segment LEDs. The cathodes are connected to scan lines through driver transistors. The display can be blanked by BD (low) line. The display section consists of 16 x 8 display RAM. The CPU can read from or write into any location of the display RAM.

SCAN SECTION:

The scan section has a scan counter and four scan lines, SL0 to SL3. In decoded scan mode, the output of scan lines will be similar to a 2-to-4 decoder. In encoded scan mode, the output of scan lines will be binary count, and so an external decoder should be used to convert the binary count to decoded output. The scan lines are common for keyboard and display. The scan lines are used to form the rows of a matrix keyboard and also connected to digit drivers of a multiplexed display, to turn ON/OFF.

CPU INTERFACE SECTION:

The CPU interface section takes care of data transfer between 8279 and the processor. This section has eight bidirectional data lines DB0 to DB7 for data transfer between 8279 and CPU. It requires two internal address A =0 for selecting data buffer and A = 1 for selecting control register of 8279.

The control signals WR (low), RD (low), CS (low) and A0 are used for read/write to 8279. It has an interrupt request line IRQ, for interrupt driven data transfer with processor.

The 8279 require an internal clock frequency of 100 kHz. This can be obtained by dividing the input clock by an internal prescaler. The RESET signal sets the 8279 in 16-character display with two -key lockout keyboard modes.

8279 − PIN DESCRIPTION

The following Figure 3.6.2 shows the pin diagram of 8279.

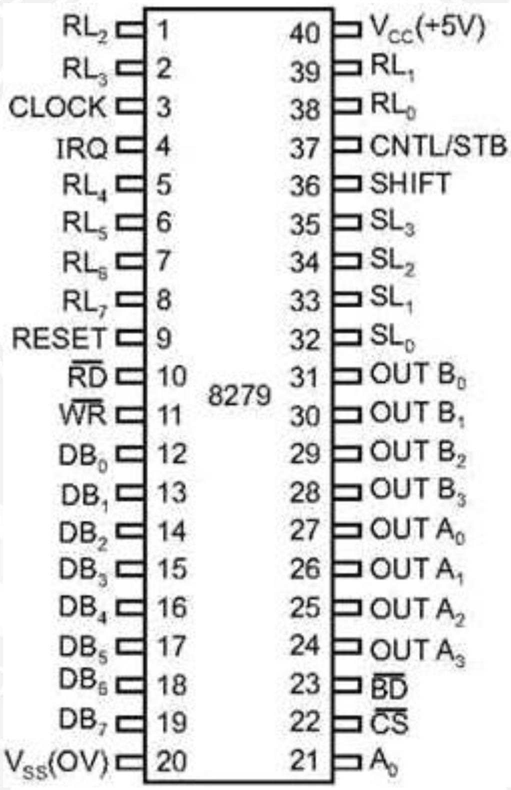


Figure 3.6.2 Pin Configuration of Keyboard display controller

[Source: Advanced Microprocessors and Microcontrollers by A.K Ray & K.M.Bhurchandi]

Data Bus Lines, DB0 - DB7

These are 8 bidirectional data bus lines used to transfer the data to/from the CPU.

CLK

The clock input is used to generate internal timings required by the microprocessor.

RESET

This pin is used to reset the microprocessor.

CS (Chip Select)

When this pin is set to low, it allows read/write operations, else this pin should be set to high.

A0

This pin indicates the transfer of command/status information. When it is low, it indicates the transfer of data.

RD, WR

This Read/Write pin enables the data buffer to send/receive data over the data bus.

IRQ

This interrupt output line goes high when there is data in the FIFO sensor RAM. The interrupt line goes low with each FIFO RAM read operation. However, if the FIFO RAM further contains any key-code entry to be read by the CPU, this pin again goes high to generate an interrupt to the CPU.

Vss, Vcc

These are the ground and power supply lines of the microprocessor.

SL0 − SL3

These are the scan lines used to scan the keyboard matrix and display the digits. These lines can be programmed as encoded or decoded, using the mode control register.

RL0 − RL7

These are the Return Lines which are connected to one terminal of keys, while the other terminal of the keys is connected to the decoded scan lines. These lines are set to 0 when any key is pressed.

SHIFT

The Shift input line status is stored along with every key code in FIFO in the scanned keyboard mode. Till it is pulled low with a key closure, it is pulled up internally to keep it high

CNTL/STB - CONTROL/STROBED I/P Mode

In the keyboard mode, this line is used as a control input and stored in FIFO on a key closure. The line is a strobe line that enters the data into FIFO RAM, in the strobed input mode. It has an internal pull up. The line is pulled down with a key closure.

BD

It stands for blank display. It is used to blank the display during digit switching.

OUTA0 – OUTA3 and OUTB0 – OUTB3

These are the output ports for two 16x4 or one 16x8 internal display refresh registers. The data from these lines is synchronized with the scan lines to scan the display and the keyboard.

3.7 INTERRUPT CONTROLLER

PROGRAMMABLE INTERRUPT CONTROLLER- INTEL 8259A

The 8259A is a programmable interrupt controller specially designed to work with Intel microprocessor 8080, 8085A, 8086, 8088. The main features of 8259A programmable interrupt controller are as follows:

- It can handle eight interrupt inputs. This is equivalent to providing eight interrupt pins on the processor in place of one INT pin.
- It can resolve eight levels of interrupt priorities in a variety of modes.
- Each of the interrupt requests can be masked individually.
- The status of pending interrupts, in service interrupts, and masked interrupts can be read atany time.
- The chip can be programmed to accept interrupt requests either as level triggered or edgetriggered interrupt request.

PIN CONFIGURATION OF INTEL 8259A

The 8259 A is contained in a 28 dual-in-line package that requires only +5V supply voltage. It also includes additional features such aslevel triggered mode, buffered mode and automatic end of interrupt mode.The pin diagram and internal block diagram of PIC is shown in Figure 3.7.1. The pins are defined as follows:

CS (Chip Select signal):

To access this chip, chip select signal CS is made low. A LOW on this pin enables RD & WR communication between the CPU and the 8259A. This signal is made LOW by decoding the addresses through the decoder logic circuit. Interrupt acknowledge functions to transfer the control to interrupt service subroutine are independent of CS.

WR (Write signal)**:**

A low on this pin enables the 8259 A to accept command words from CPU.

RD (Read signal):

A low on this pin enables this 8259A to release status (pending interrupts or in-service interrupts or masked interrupts) on to the data bus for the CPU. The status includes the contents of IMR (interrupt mask register) or ISR (interrupt service register) or IRR (interrupt request register) or a priority level.

D7-D0 (Data Bus):

Control, status and interrupt vector information are transferred via this Bidirectional data bus.

CAS2-CAS0 (Cascade lines):

The CAS2-0 lines form a local 8259A bus to control multiple 8259As in master-slave configuration, i.e., to identify a particular slave 8259A to be accessed for transfer of vector information. These pins are automatically set as output pins for master 8259A and input pins for a slave 8259A once the chips are programmed as master or slave.

SP/ EN (Salve Program/Enable Buffer):

This is a dual function pin. When the chip is programmed in buffered mode, the pin can be used as an output and when not in the buffered mode it is used as an input. In non-buffered mode it is used as an input pin to determine whether the 8259A is to be used as a master (SP/ EN = 1) or as a slave (SP/ EN =0).

INT (Interrupt output):

This pin goes high whenever a valid interrupt request is asserted. It is used to interrupt the CPU, thus it is connected to the CPU's interrupt pin (INT). In case of master-slave configuration, the interrupt pin of slave 8259A is connected to interrupt request input of master 8259A.

INTA (Interrupt Acknowledge):

This pin is used to enable 8259A interrupt vector data on the data bus by a sequence of interrupt acknowledge pulses issued by the CPU.

IR0-IR7 (Interrupt Request inputs):

These are asynchronous interrupt request input pins. An interrupt request is executed by raising an IR input (low to high), and holding it high until it is acknowledged. (Edge triggered mode) or just by a high level on an interrupt request input (Level triggered mode).

A0 (A0 address line):

This pin acts in conjunction with the RD, WR & CS pins. It is used by the 8259A to send various command words from the CPU and to read the status. It is normally connected to the CPU A0 address line. Two addresses are assigned/ reserved in the I/O address space for each 8259A in the system- one with A0 =0 is called even address and other with A0 = 1is called odd address.

FUNCTIONAL DESCRIPTION :

The 8259A (PIC) has eight interrupt request inputs – IR7 - IR0. The 8259A uses its INT output to interrupt the 8086 via INT pin. The 8259A receives interrupt acknowledge pulses from the CPU at its INTA input. Vector address, used by the 8086 to transfer the control to the service subroutine of the interrupting device, is provided by the 8259A on the data bus. The 8259A is a programmable device that must be initialized by command words sent by the microprocessor. After initialization the 8259A mode of operation can be changed by operation command words from the microprocessor.

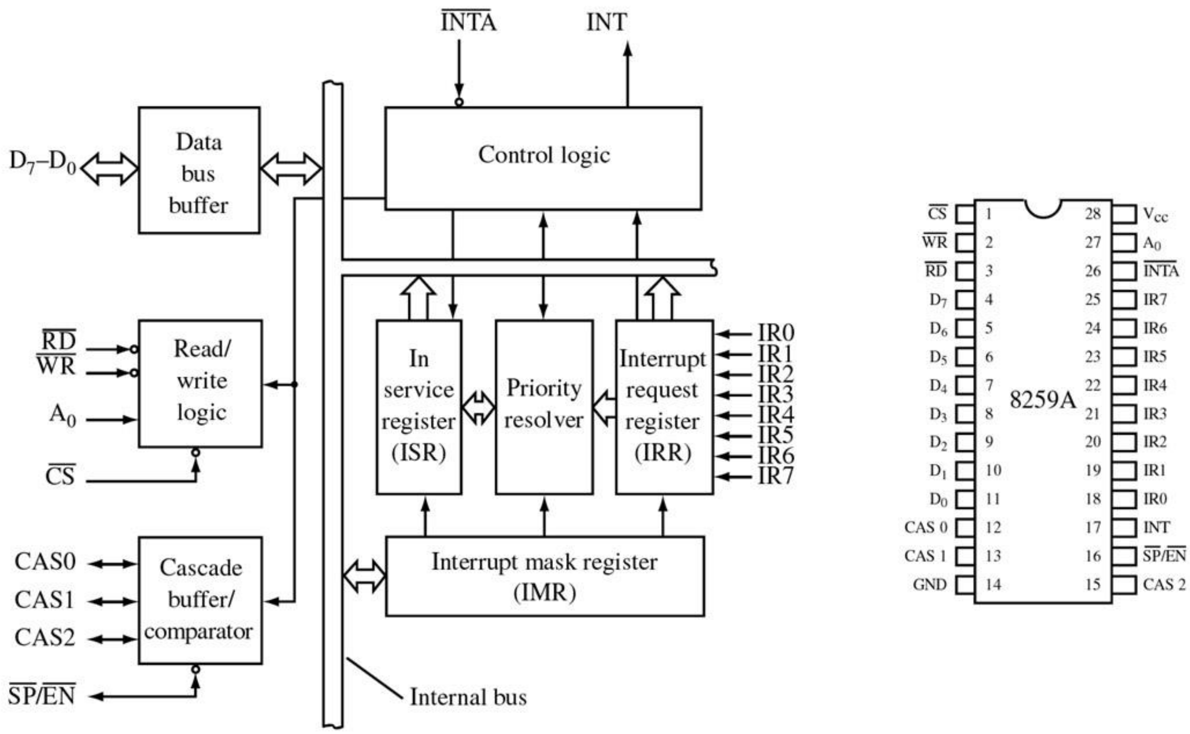


Figure 5.7.1 Block Diagram and Pin Configuration of Intel 8259A

[Source: Advanced Microprocessors and Microcontrollers by A.K Ray & K.M.Bhurchandi]

8259 contains following blocks-

Data bus buffer-

It is used to transfer data between microprocessor and internal bus.

Read/write logic-

- It sets the direction of data bus buffer.
- It controls all internal read/write operations.
- It contains initialization and operation command registers.

Cascaded buffer and comparator-

- In master mode, it functions as a cascaded buffer. The cascaded buffers output slave identification number on cascade lines.

- In slave mode, it functions as a comparator. The comparator reads slave identification number from cascade lines and compares this number with its internal identification number.
- In buffered mode, it generates an (EN) signal.

Control logic

It generates an INT signal. In response to an (INTA) signal, it releases three byte CALL address or one byte vector number.

- It controls read/write control logic, cascade buffer/comparator, in service register, priority resolver and IRR.

Interrupt request register-

- It is used to store all pending interrupt requests.
- Each bit of this register is set at the rising edge or at the high level of the corresponding interrupt request line.
- The microprocessor can read contents of this register by issuing appropriate command word.

In service register (ISR)

- It is used to store all interrupt levels currently being serviced.
- Each bit of this register is set by priority resolver and reset by end of interrupt command word.
- The microprocessor can read contents of this register by issuing appropriate command word.

Priority resolver

- It determines the priorities of the bit set in the IRR. To make decision, the priority resolver looks at the ISR.
- If the higher priority bit in the ISR is set, then it ignores the new request.
- If the priority resolvers find that the new interrupt has a higher priority than the highest priority interrupt currently being serviced and the new interrupt is not in service, then it will set appropriate bit in the ISR and send the INT signal to the microprocessor for new interrupt request.

Interrupt mask register (IMR)

- It is used to mask unwanted interrupt request by writing appropriate command word.
- The microprocessor can read contents of this register without issuing any command word.

Interrupt sequence

The powerful features of the 8259A in a microcomputer system are its programmability and the interrupt routine addressing capability. The latter allows direct or indirect jumping to the normal sequence of events during an interrupt depends on the type of CPU being used. The events occur as follows:

1. One or more of the INTERRUPT REQUEST lines (IR7-IR0) are raised high, setting the corresponding IRR bit(s).

2. The 8259A evaluates these requests, and sends an INT to the CPU, if appropriate.

3. The CPU acknowledges the INT and responds with an INTA pulse.

4. This CALL instruction will initiate two more INTA pulses to be sent to the 8259A from the CPU.

5. These two INTA pulses allow the 8259A to release its preprogrammed subroutine address onto the Data Bus. The lower 8-bit address is released at the first INTA pulse and the higher 8-bit address is released at the second INTA pulse.

6. This completes the 3-byte CALL instruction released by the 8259A. In the AEOI mode the ISR bit is reset at the end of the third INTA pulse. Otherwise, the ISR bit remains set until an appropriate EOI command is issued at the end of the interrupt sequence.

7. Upon receiving an INTA from the CPU, the highest priority ISR bit is set and the corresponding IRR bit is reset.

8. The 8086 will initiate a second INTA pulse. During this pulse, the 8259A releases an 8-bit pointer onto the Data Bus where it is read by the CPU.

9. This completes the interrupt cycle.

3.8 DIRECT MEMORY ACCESS (DMA) CONTROLLER (8257):

It is designed by Intel to transfer data at the fastest rate. It allows the device to transfer the data directly to/from memory without any interference of the CPU. Using a DMA controller, the device requests the CPU to hold its data, address and control bus, so the device is free to transfer data directly to/from the memory. The DMA data transfer is initiated only after receiving HLDA signal from the CPU.

The sequences of operations performed by a DMA are

- Initially, when any device has to send data to the memory, the device has to send DMA request (DRQ) to DMA controller.
- The DMA controller sends Hold request (HRQ) to the CPU and waits for the CPU to assert the HLDA signal.
- Then the microprocessor tri-states all the data bus, address bus, and control bus. The CPU will relinquish the bus and acknowledges the HOLD request through HLDA signal.
- Now the CPU is in HOLD state and the DMA controller has to manage the operations over buses between the memory interfaced with Microprocessor and I/O devices.

FEATURES OF 8257

- It has four channels that can be used over four I/O devices.
- Each channel has 16-bit address and 14-bitcounter.
- Each channel can transfer data up to64kb.
- Each channel can be programmed independently.
- Each channel can perform read transfer, write transfer and verify transfer operations.
- It operates in 2 modes, i.e., **Master mode** and **Slave mode**.

8257 PIN DESCRIPTION

The pin configuration of DMA Controller (8257) is shown in Figure 3.8.1 and the descriptions are as follows:

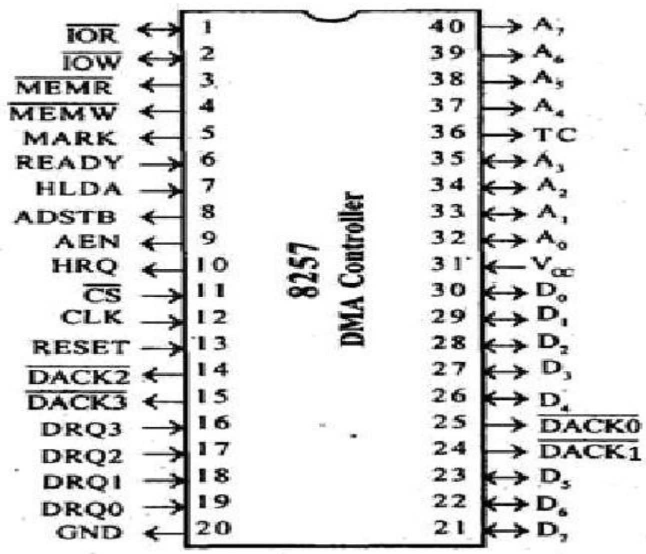


Figure 3.8.1 Pin Configuration of 8257

[Source: Advanced Microprocessors and Microcontrollers by A.K Ray & K.M.Bhurchandi]

DRQ0−DRQ3

These are the four individual channel DMA request inputs, which are used by the peripheral devices for using DMA services. When the fixed priority mode is selected, then DRQ0 has the highest priority and DRQ3 has the lowest priority.

DACKo − DACK3

These are the active-low DMA acknowledge lines, which updates the requesting peripheral about the status of their request by the CPU. These lines can also act as strobe lines for the requesting devices.

Do − D7

These are bidirectional, data lines which are used to interface the system bus with the internal data bus of DMA controller. In the Slave mode, it carries command words to 8257 and status word from 8257. In the master mode, these lines are used to send higher byte of the generated address to the latch. This address is further latched using ADSTB signal.

IOR

It is an active-low bidirectional tri-state input line, which is used by the CPU to read internal registers of 8257 in the Slave mode. In the master mode, it is used to read data from the peripheral devices during a memory write cycle.

IOW

It is an active low bi-direction tri-state line, which is used to load the contents of the data bus to the 8-bit mode register or upper/lower byte of a 16-bit DMA address register or terminal count register. In the master mode, it is used to load the data to the peripheral devices during DMA memory read cycle.

CLK

It is a clock frequency signal which is required for the internal operation of 8257.

RESET

This signal is used to RESET the DMA controller by disabling all the DMA channels.

Ao - A3

These are the four least significant address lines. In the slave mode, they act as an input, which selects one of the registers to be read or written. In the master mode, they are the four least significant memory address output lines generated by8257.

CS

It is an active-low chip select line. In the Slave mode, it enables the read/write operations to/from 8257. In the master mode, it disables the read/write operations to/from 8257.

READY

It is an active-high asynchronous input signal, which makes DMA ready by inserting wait states.

HRQ

This signal is used to receive the hold request signal from the output device. In the slave mode, it is connected with a DRQ input line 8257. In Master mode, it is connected with HOLD input of the CPU.

HLDA

It is the hold acknowledgement signal which indicates the DMA controller that the bus has been granted to the requesting peripheral by the CPU when it is set to1.

MEMR

It is the low memory read signal, which is used to read the data from the addressed memory locations during DMA read cycles.

MEMW

It is the active-low three state signal which is used to write the data to the addressed memory location during DMA write operation.

ADSTB

It is a control output line used to split data and address line through Latches.

AEN

This signal is used to disable the address bus/data bus.

TC

It stands for ‘Terminal Count’, which indicates the present DMA cycle to the present peripheral devices.

MARK

The mark will be activated after each 128 cycles or integral multiples of it from the beginning. It indicates the current DMA cycle is the 128th cycle since the previous MARK output to the selected peripheral device.

Vcc

It is the power signal which is required for the operation of the circuit.

INTERNAL ARCHITECTURE OF 8257:

The functional Block Diagram of DMA controller(8257) is shown in Figure 3.8.2 and the description are as follows: It consists of five functional blocks:

a) Data bus buffer

b) Control logic

c) Read/write logic

d) Priority Resolver

e) DMA channels

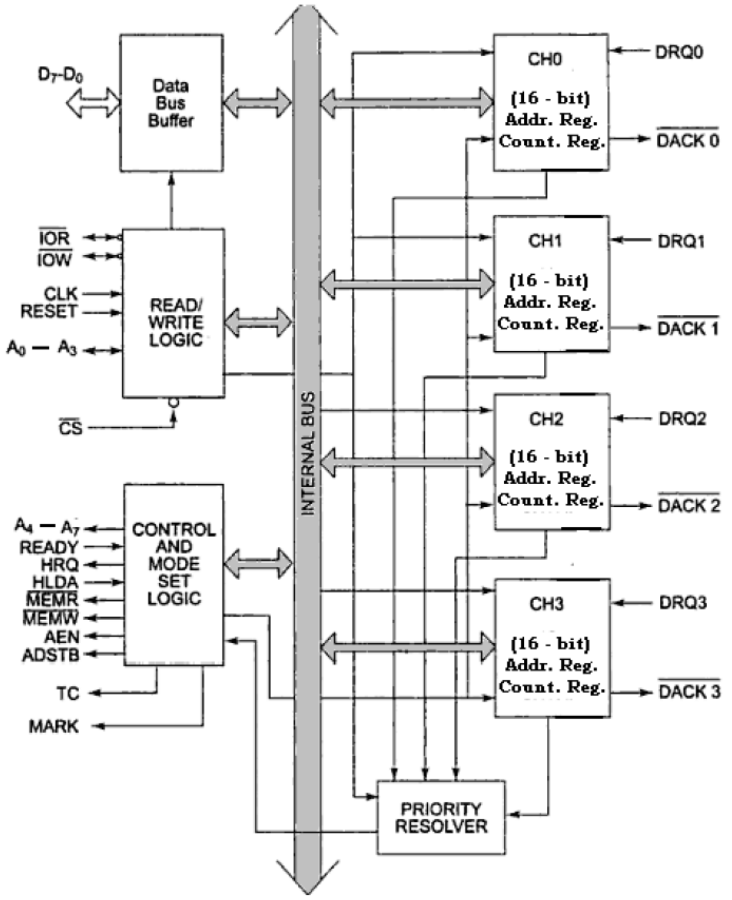


Figure 3.8.2 Functional Block Diagram of 8257

[Source: Advanced Microprocessors and Microcontrollers by A.K Ray & K.M.Bhurchandi]

Data Bus Buffer:

8-bit Tristate, bidirectional buffer interfaces the internal bus of 8257 with the external system bus under the control of various control signals.

Read/Write Logic:

In the slave mode, the read/write logic accepts the I/O Read or I/O Write signals, decodes the Ao-A3 lines and either writes the contents of the data bus to the addressed internal register or reads the selected register depending upon whether IOW or IOR signal is activated.In master mode, the read/write logic generates the IOR and IOW signals to control the dataflow to or from the selected peripheral.

Control Logic:

The control logic controls the sequences of operations and generates the required control signals like AEN, ADSTB, MEMR,MEMW, TC and MARK along with the address lines A4-A7, in master mode.

Priority Resolver:

The priority resolver resolves the priority of the four DMA channels depending upon whether normalpriority or rotating priority is programmed.

Register Organisation of 8257:

The 8257 performs DMA operation over four independent DMA channels with the following Registers.

1. **DMA Address Register**

Each DMA channel has one DMA address register. The function of this register is to store theaddress of the starting memory location, which will be accessed by the DMA channel. The device that wants to transfer data over a DMA channel, will access the block of the memory with the starting addressstored in the DMA Address

Register.

2. **Terminal Count Registers**

Each of the four DMA channels of 8257 has one terminal count register (TC). This 16-bit register is used for ascertaining that the data transfer through a DMA channel ceases or stops after the required number of DMA cycles.

After each DMA cycle, the terminal count register content will be decremented by one and finally it becomes zero after the required number of DMA cycles are over.The bits 14 and 15 of this register indicate the type of the DMA operation (transfer).

3. **Mode Set Register**

The mode set register is used for programming the 8257 as per the requirements of the system. The function of the mode set register is to enable the DMA channels individually and also to set the various modes of operation as shown in Figure 3.8.3.

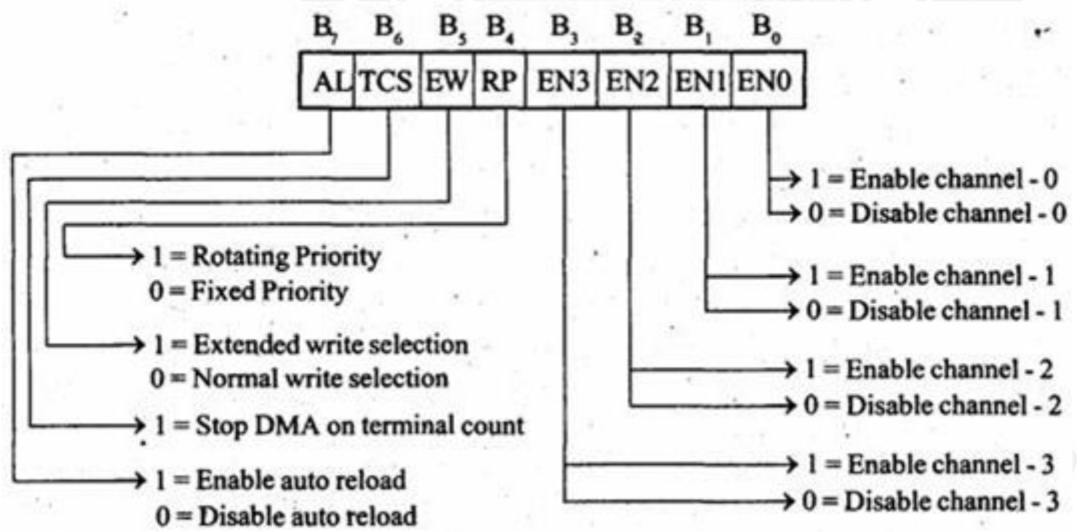


Figure 3.8.3 Mode Set Register

[Source: Advanced Microprocessors and Microcontrollers by A.K Ray & K.M.Bhurchandi]

The bits Do-D3 enable one of the four DMA channels of 8257.If the TC STOP bit is set, the selected channel is disabled after the terminal count condition is reached, and it further prevents any DMA cycle on the channel. If the TC STOP bit is programmed to be zero, the channel is not disabled, even after the countreaches zero and further request are allowed on the same channel. The auto load bit, if set, enables channel 2 for the repeat block chaining operations, without immediate software intervention between the two successive blocks. The extended write bit, if set to '1', extends the duration of MEMW and IOW signals by activatingthem earlier, which is useful in interfacing the peripherals with different access times.

4. **Status register**

The lower order 4-bits of this register contain the terminal count status for the four individual channels.If any of these bits is set, it indicates that the specific channel has reached the terminal count condition. The update flag is not affected by the read operation. This flag can only be cleared by resetting 8257. The update flag is set every time, the channel 2 registers are loaded with contents of the channel 3 registers. It is cleared by the completion of the first DMA cycle of the new block. This register can onlyread.

DMA TRANSFER & OPERATIONS

The 8257 is able to accomplish three types of operations suchas

1.DMA operation
2. Write Operation
3. Read Operation

Operational sequence of 8257 is as follows

- The 8257 request any one of the 8257 DRQ inputs to transfer single byte.
- In response to the request, the 8257 sends HRQ signal to CPU at its HLD input and waitsfor acknowledgement at the HLDA input.
- If the DMA controller receives the HLDA signal it indicates that the bus is available for the transfer.
- The DMA controller generate the read and write commands to transfer the

byte from/to the I/O Device.

- The DACK line of the used channel is pulled down by the DMA controller to I/O device that requested for DMA transfers.
- The HRQ line is lowered by the DMA controller to indicate the CPU that it may regain the control of the bus.
- The DRQ must be high until acknowledged.
- In each s4 state ,the DRQ lines are sampled and highest priority request is recognized during next transfer. The HRQ line is maintained active till all the DRQ line go low.