## 5.5 PN JUNCTION:

PN junction diode is a 2 terminal polarity sensitive device. The diode conducts when forward bias is applied and it will introduce zero resistance in the circuit. The diode does not conduct when reverse bias is applied and it will introduce infinite resistance in the circuit, is shown in Fig 5.5.1.

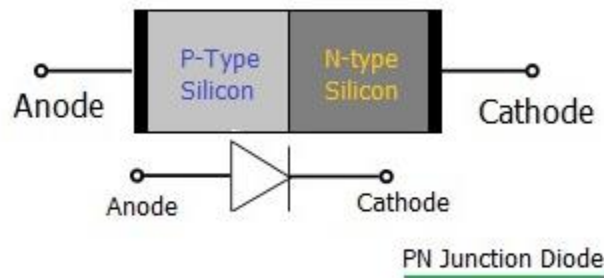


**Fig : 5.5.1 PN Diode symbol**

**[Source: Reinhold Ludwig and Powel Bretchko,‖ RF Circuit Design – Theory and Applications, Page-279]**

It is made up of P-type silicon and N-type silicon semiconductor materials. The current is commonly known as a diffusion current and is composed of electrons end holes in Fig 5.5.2.

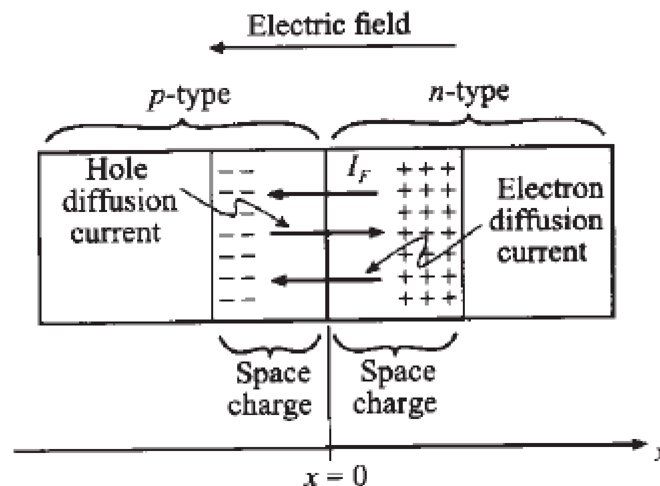


**Fig : 5.5.2 Current flow in the PN-junction**

**[Source: Reinhold Ludwig and Powel Bretchko,‖ RF Circuit Design – Theory and Applications, Page-279]**

For applications where high currents and high voltages are used, neither the alloy nor the grown junction diodes were satisfactory because of voltage and current limitations respectively. A new type of diode was invented for high, power applications . This diode is made from a die of very nearly pure intrinsic silicon which has a very high resistivity. A P type and an N type impurity are diffused into the intrinsic material on either side of the die. This makes the PIN or P+ it N+ configuration sketched in Figure 10a. Figure 10b shows the variation of doping level for this diode which is directly proportional to the conductivity as a function of distance through the diode. Thus the N and P regions are high conductivity or low resistivity regions, and the I region is a low conductivity region.

For the purposes of this section, an ideal diode is defined as a diode with a voltage current characteristic as given by equation 4. This equation relates the current through a semiconductor diode to the voltage externally applied to it.

$$I = I_S \left[ e^{\left(\frac{qV}{kT}\right) - 1} \right]$$

where I is the temperature sensitive saturation current given in equation 3, kT is a voltage equivalent of temperature which is 0.026 volt at room q temperature, and V and I are the voltage across the diode and the current through it respectively with polarities and current directions defined in Figure 8. Die symbol V is substituted for VA for simplification. Equation 5 and 6 represent the V-I characteristic for the forward biased and the reverse biased situations. These equations hold for values of applied voltage greater than 0.1 volt at useful temperatures.

$$I = I_S e^{\left(\frac{qV}{kT}\right)}$$

$$I = -I_S$$

The ideal diode presents a purely resistive component of impedance to an a-c signal since equation 4 allows for no frequency effects. For a small signal situation the instantaneous voltage applied to the diode

v = $V_O$ + v cos$\omega t$

where $V_O$ is the d-c bias voltage and v is the peak amplitude of the small a-c signal. For small signal applications v <•< $V_O$.

I = $I_S + \frac{dI}{dV}$ cos$\omega t$

where I is the instantaneous current, $I_o$ is equal to $I_B\ e^{\left(\frac{qV}{kT}\right)}$and $\frac{dI}{dV}$ a conductance evaluated at V equal to $V_O$. Equation is valid for small a-c voltages only since the higher order terms of the Taylor series expansion are neglected. The current I can be written as

I = $I_O$ + i cos$\omega t$

where i is the peak value of the a-c current, and equation 10 gives the relationship between i and v.

i = $\frac{dI}{dV}$ v = gV

The conductance g is a small signal a-c conductance relating the a-c current and voltage. The approach outlined above allows the analysis of ideal semiconductor diodes to be performed in two distinct steps. First the d-c bias conditions are analyzed followed by the computation of the a-c operating conditions using the small signal conductance g.

**SCHOTTKY DIODE:**

The diode is constructed on a thin silicon(n+ type) substrate by growing epitaxially on n-type active layer of about 2 micron thickness. A thin SiO2 layer is grown thermally over this active layer. Metal semiconductor junction is formed by depositing metal over SiO2 in Fig 5.5.3.

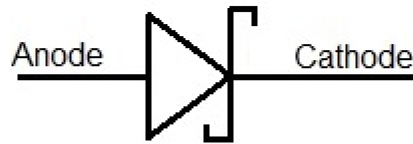


**Fig: 5.5.3 Schottky diode symbol**

**[Source: Reinhold Ludwig and Powel Bretchko,‖ RF Circuit Design – Theory and Applications, Page-289]**

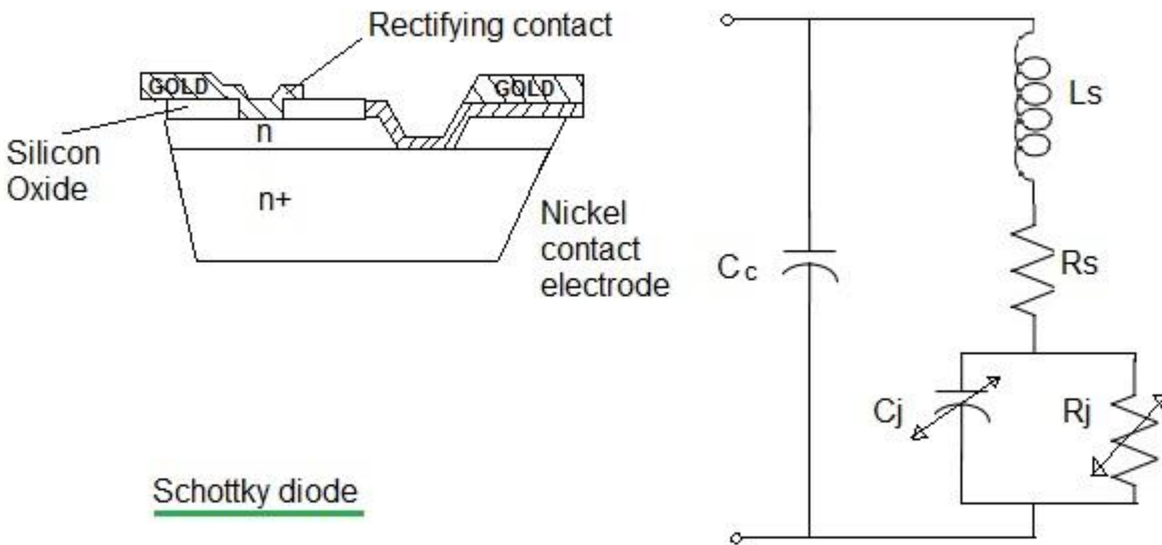


Fig: 5. 5.4 Schottky diode contact

**[Source: Reinhold Ludwig and Powel Bretchko,‖ RF Circuit Design – Theory and Applications, Page-290]**

When the schottky diode is forward biased, the major carriers (i.e. electrons) can be easily injected from highly doped n-semiconductor material into the metal.

When it is reverse biased, the barrier height becomes too high for the electrons to cross and no conduction will happen. These applications are very useful.
In Fig 5.5.41, RF power flow in the device is limited by power dissipation in Rs. It is shorted across Cj, Cc and Ls. These will produce RF mismatch and can be matched by external circuit.