BIST

- Only clocked D-type master-slave flip-flops for all state variables should be used.
- At least one PI pin must be available for test. It is better if more pins are available.
- All clock inputs to flip-flops must be controlled from primary inputs (PIs). There will be no gated clock. This is necessary for FFs to function as a scan register.
- Clocks must not feed data inputs of flip-flops. A violation of this can lead to a race condition in the normal mode.

BIST Overheads

The use of scan design produces two types of overheads. These are area overhead and performance overhead. The scan hardware requires extra area and slows down the signals.

- **IO pin overhead:** At least one primary pin necessary for test.
- **Area overhead:** *Gate overhead* = [4 $n_{sff}/(n_g+10n_{ff})$] x 100%, where n_g = number of combinational gates; n_{ff} = number of flip-flops; n_{sff} = number of scan flip-flops; For full scan number of scan flip-flops is equal to the number of original circuit flip-flops. Example: n_g = 100k gates, n_{ff} = 2k flip-flops, overhead = 6.7%. For more accurate estimation scan wiring and layout area must be taken into consideration.
- **Performance overhead:** The multiplexer of the scan flip-flop adds two gate-delays in combinational path. Fanouts of the flip-flops also increased by 1, which can increase the clock period.

Scan Variations

There have been many variations of scan as listed below, few of these are discussed here.

- MUXed Scan
- Scan path
- Scan-Hold Flip-Flop

- Serial scan
- Level-Sensitive Scan Design (LSSD)
- Scan set
- Random access scan

MUX Scan

- It was invented at Stanford in 1973 by M. Williams & Angell.
- In this approach a MUX is inserted in front of each FF to be placed in the scan chain.

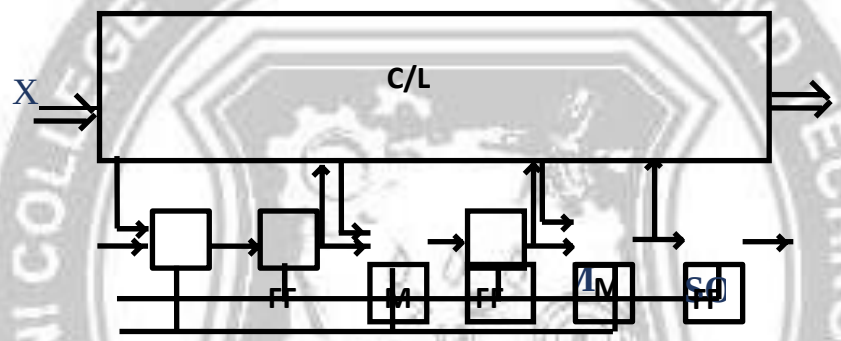

Fig. 5.4.1 The Shift-Register Modification approach

[Source: R.Jacob Baker, Harry W.LI., David E.Boyee, ―CMOS Circuit Design, Layout and Simulation]

- Fig. 39.2 shows that when the test mode pin T=0, the circuit is in normal operation mode and when T=1, it is in test mode (or shift-register mode).
- The scan flip-flips (FFs) must be interconnected in a particular way. This approach effectively turns the sequential testing problem into a combinational one and can be fully tested by compact ATPG patterns.
- There are two types of overheads associated with this method. The hardware overhead due to three extra pins, multiplexers for all FFs, and extra routing area. The performance overhead includes multiplexer delay and FF delay due to extra load.

Scan Path

- This approach is also called the Clock Scan Approach.
- It was invented by Kobayashi *et al*. in 1968, and reported by Funatsu *et al*. in 1975, and adopted by NEC.
- In this approach multiplexing is done by two different clocks instead of a MUX.
- It uses two-port raceless D-FFs as shown in Figure 39.3. Each FF consists of two latches operating in a master-slave fashion, and has two clocks (C1 and C2) to control the scan input (SI) and the normal data input (DI) separately.
- The two-port raceless D-FF is controlled in the following way:
- For normal mode operation C2 = 1 to block SI and C1 = 0 →1 to load DI.
- For shift register test mode C1 = 1 to block DI and C2 = 0 →1 to load SI.

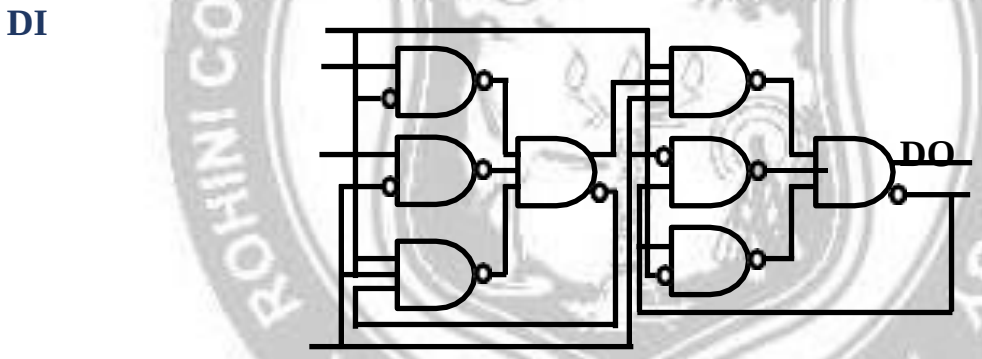

Fig.5.4.2: Logic diagram of the two-port raceless D-FF

[Source: R.Jacob Baker, Harry W.LI., David E.Boyee, ―CMOS Circuit Design, Layout and Simulation]

- This approach gives a lower hardware overhead (due to dense layout) and less performance penalty (due to the removal of the MUX in front of the FF) compared to the MUX Scan Approach. The real figures however depend on the circuit style and technology selected, and on the physical implementation.

Scan-Based Techniques

The controllability and observability can be enhanced by providing more accessible logic nodes with use of additional primary input lines and multiplexors.However, the use of additional I/O pins can be costly not only for chip fabrication but also for packaging. A popular alternative is to use scan registers with both shift and parallel load capabilities. The scan design technique is a structured approach to design sequential circuits for testability.

The storage cells in registers are used as observation points, control points, or both. By using the scan design techniques, the testing of a sequential circuit is reduced to the problem of testing a combinational circuit.In general, a sequential circuit consists of a combinational circuit and some storage elements. In the scan-based design, the storage elements are connected to form a long serial shift register, the so-called scan path, by using multiplexors and a mode (test/ normal) control signal, as shown in Fig. 1 .In the test mode, the scan-in signal is clocked into the scan path, and the output of the last stage latch is scanned out. In the normal mode, the scan-in path is disabled and the circuit functions as a sequential circuit. The testing sequence is as follows:

Step 1: Set the mode to test and, let latches accept data from scan-in input.
Step 2: Verify the scan path by shifting in and out the test data.
Step 3: Scan in (shift in) the desired state vector into the shift register.
Step 4: Apply the test pattern to the prim ary input pins.
Step 5: Set the mode to normal and observe the primary outputs of the circuit after sufficient time for propagation.,
Step 6: Assert the circuit clock, for one machine cycle to capture the outputs of the combinational logic into the registers.
Step 7: Return to test mode; scan out the contents of the registers, and at the same time scan in the next pattern.
Step 8: Repeat steps 3-7 until all test patterns are applied.

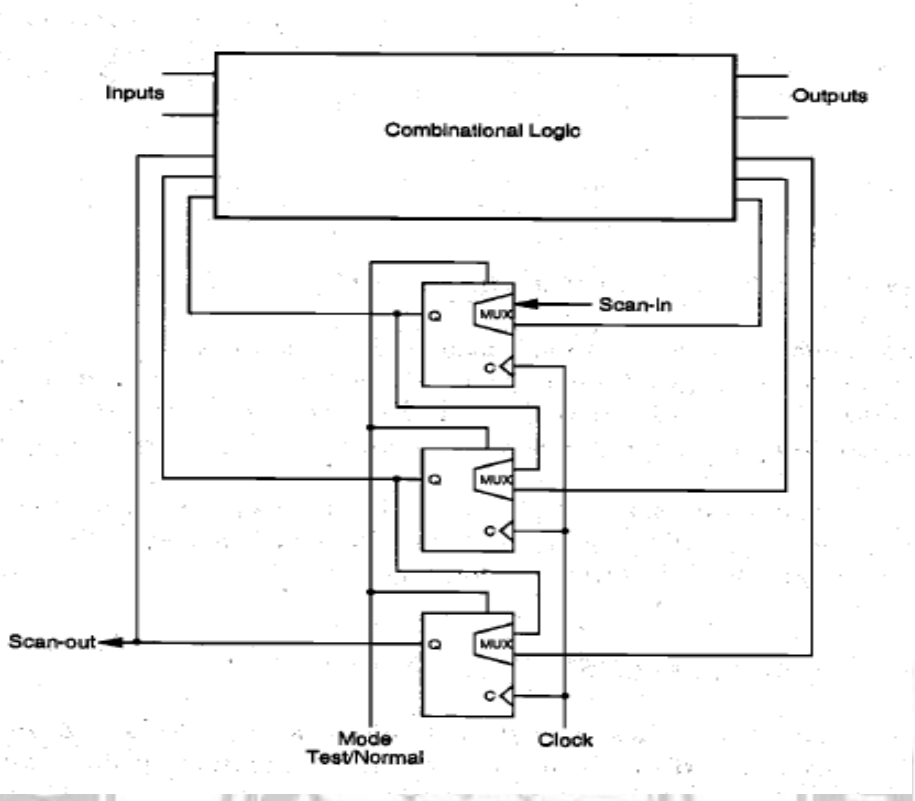

Figure 5.4.3: The general structure of scan-based design

[Source: R.Jacob Baker, Harry W.LI., David E.Boyee, ―CMOS Circuit Design, Layout and Simulation]

The storage cells in scan design can be implemented using edge-triggered D flipflops, master-slave flip-flops, or level-sensitive latches controlled by complementary clock signals to ensure race-free operation. Figure 2 shows a scan-based design of an edge-triggered D flip-flop. In large high-speed circuits, optimizing a single clock signal for skews, etc., both for normal operation and for shift operation, is difficult. To overcome this difficulty, two separate clocks, one for normal operation and one for shift operation, are used. Since the shift operation does not have to be performed at the target speed, its clock is much less constrained.

An important approach among scan-based designs is the level sensitive scan design (LSSD), which incorporates both the level sensitivity and the scan path approach using shift registers. The level sensitivity is to ensure that the sequential circuit response is independent of the transient characteristics of the circuit, such as the component and wire delays. Thus, LSSD removes hazards and races. Its ATPG is also simplified since tests have to be generated only for the combinational part of the circuit.

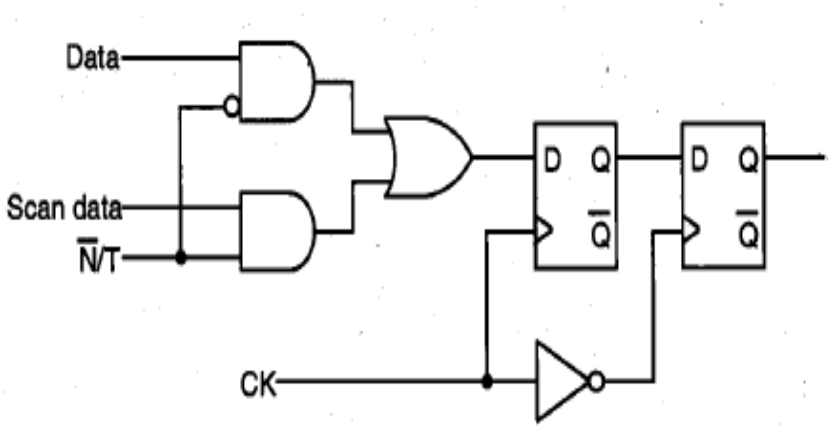

Figure 5.4.4: Scan-based design of an edge-triggered D flip-flop

[Source: R.Jacob Baker, Harry W.LI., David E.Boyee, ―CMOS Circuit Design, Layout and Simulation]

The boundary scan test method is also used for testing printed circuit boards (PCBs) and multichip modules (MCMs) carrying multiple chips. Shift registers are placed in each chip close to I/O pins in order to form a chain around the board for testing. With successful implementation of the boundary scan method, a simpler tester can be used for PCB testing.

On the negative side, scan design uses more complex latches, flip-flops, I/O pins, and interconnect wires and, thus, requires more chip area. The testing time per test pattern is also increased due to shift time in long registers.

Level-Sensitive Scan Design (LSSD)

- This approach was introduced by Eichelberger and T. Williams in 1977 and 1978.
- It is a latch-based design used at IBM.
- It guarantees race-free and hazard-free system operation as well as testing.
- It is insensitive to component timing variations such as rise time, fall time, and delay. It is faster and has a lower hardware complexity than SR modification.
- It uses two latches (one for normal operation and one for scan) and three clocks. Furthermore, to enjoy the luxury of race-free and hazard-free system operation and test, the designer has to follow a set of complicated design rules.
- A logic circuit is *level sensitive* (LS) iff the steady state response to any allowed input change

is independent of the delays within the circuit. Also, the response is independent of the order in which the inputs change

LSSD requires that the circuit be LS, so we need LS memory elements as defined above. Figure 39.4 shows an LS polarity-hold latch. The correct change of the latch output (L) is not dependent on the rise/fall time of C, but only on C being `1' for a period of time greater than or equal to data propagation and stabilization time. Figure 39.5 shows the polarity-hold shift-register latch (SRL) used in LSSD as the scan cell.

The scan cell is controlled in the following way:

- Normal mode: A=B=0, C=0 □ 1.
- SR (test) mode: C=0, AB=10□ 01 to shift SI through L_1 and L_2.

Advantages of LSSD

1. Correct operation independent of AC characteristics is guaranteed.
2. FSM is reduced to combinational logic as far as testing is concerned.
3. Hazards and races are eliminated, which simplifies test generation and fault simulation.

Drawbacks of LSSD

1. Complex design rules are imposed on designers. There is no freedom to vary from the overall schemes. It increases the design complexity and hardware costs (4-20% more hardware and 4 extra pins).
2. Asynchronous designs are not allowed in this approach.
3. Sequential routing of latches can introduce irregular structures.
4. Faults changing combinational function to sequential one may cause trouble, e.g., bridging and CMOS stuck-open faults.
5. Test application becomes a slow process, and normal-speed testing of the entire test sequence is impossible.
6. It is not good for memory intensive designs.

Random Access Scan

- This approach was developed by Fujitsu and was used by Fujitsu, Amdahl, and TI.
- It uses an address decoder. By using address decoder we can select a particular FF and either set it to any desired value or read out its value. Random access structure and RAM cell .
- The difference between this approach and the previous ones is that the state vector can now be accessed in a random sequence. Since neighboring patterns can be arranged so that they differ in only a few bits, and only a few response bits need to be observed, the test application time can be reduced.
- In this approach test length is reduced.
- This approach provides the ability to `watch' a node in normal operation mode, which is impossible with previous scan methods.
- This is suitable for delay and embedded memory testing.
- The major disadvantage of the approach is high hardware overhead due to address decoder, gates added to SFF, address register, extra pins and routing

Scan-Hold Flip-Flop

- Special type of scan flip-flop with an additional latch designed for low power testing application.
- The control input HOLD keeps the output steady at previous state of flip-flop.
- For HOLD = 0, the latch holds its state and for HOLD = 1, the hold latch becomes transparent.
- For normal mode operation, TC = HOLD =1 and for scan mode, TC = 1 and Hold = 0.
- Hardware overhead increases by about 30% due to extra hardware the hold latch.
- This approach reduces power dissipation and isolate asynchronous part during scan.
- It is suitable for delay test.

Partial Scan Design

- In this approach only a subset of flip-flops is scanned. The main objectives of this approach

are to minimize the area overhead and scan sequence length. It would be possible to achieve required fault coverage

- In this approach sequential ATPG is used to generate test patterns. Sequential ATPG has number of difficulties such as poor initializability, poor controllability and observability of the state variables etc. Number of gates, number of FFs and sequential depth give little idea regarding testability and presence of cycles makes testing difficult. Therefore sequential circuit must be simplified in such a way so that test generation becomes easier.
- Removal of selected flip-flops from scan improves performance and allows limited scan design rule violations.
- It also allows automation in scan flip-flop selection and test generation
  Design using partial scan architecture [1].
- Sequential depth is calculated as the maximum number of FFs encountered from PI line to PO line.

Things to be followed for a partial scan method

- A minimum set of flip-flops must be selected, removal of which would eliminate all cycles.
- Break only the long cycles to keep overhead low.
- All cycles other than self-lops should be removed.