4.1 ARCHITECTURE OF 8051

MICROCONTROLLER EVOLUTION

First, microcontrollers were developed in the mid-1970s. These were basically calculator- based processors with small ROM program memories, very limited RAM data memories and a handful of input/output ports.

As silicon technology developed, more powerful, 8-bit microcontrollers were produced. In addition to their improved instruction sets, these microcontrollers included on-chip counter/timers, interrupt facilities, and improved I/O handling. On-chip memory capacity was still small and was not adequate for many applications. One of the most significant developments at this time was the availability of on-chip ultraviolet erasable EPROM memory. This simplified the product development time considerably and for the first time, also allowed the use of microcontrollers in low-volume applications.

The 8051 family was introduced in the early 1980s by Intel. Since its introduction, the 8051 has been one of the most popular microcontrollers and has been second- sourced by many manufacturers. The 8051 currently has many different versions and some types include on-chip analogue-to-digital converters, a considerably large size of program and data memories.

INTRODUCTION TO 8051:

The **Intel MCS-51** (commonly referred to as **8051**) is a Harvard architecture, single chip microcontroller (μC) series which was developed by Intel in 1980 for use in embedded systems. The 8051 architecture provides many functions (CPU, RAM, ROM, I/O, interrupt logic, timer,etc.) in a single package

Features of 8051:

- 8-bit ALU, Accumulator, 8-bit Registers and 8-bit data bus; hence it is an 8-bit microcontroller
- 16-bit program counter
- 8-bit Processor Status Word(PSW)
- 8-bit Stack Pointer

- Internal RAM of128bytes
- On chip ROM is4KB
- Special Function Registers (SFRs) of 128bytes
- 32 I/O pins arranged as four 8-bit ports (P0 -P3)
- Two 16-bit timer/counters : T0 andT1
- Two external and three internal vectored interrupts
- Full duplex UART (serialport)

BLOCK DIAGRAM

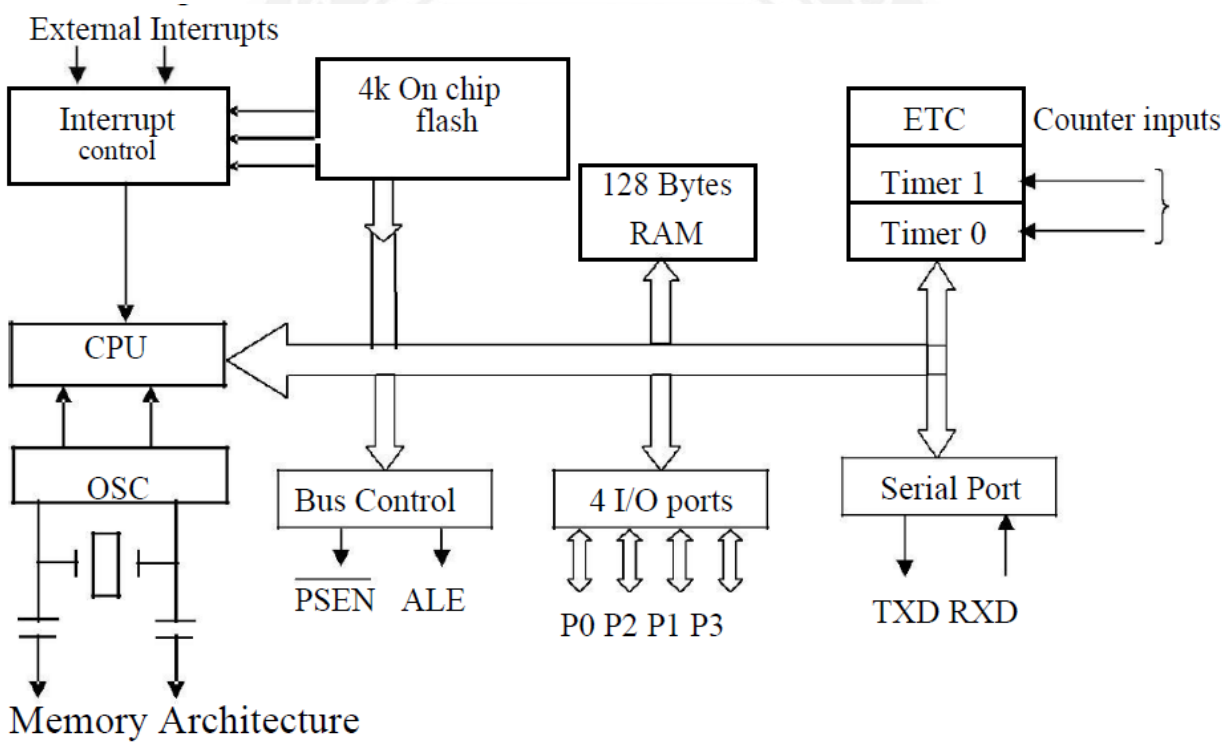

Figure 4.1.1 8051 Microcontroller Block Diagram

[Source: "The 8051Microcontroller and Embedded Systems: Using Assembly and C" by Mohamed Ali Mazidi, Janice Gillispie Mazidi, Rolin McKinlay , pg.no.29]

128 BYTES OF INTERNAL RAM STRUCTURE (LOWER ADDRESS SPACE)

30H-7FH	**Scratch Pad**	**80 Bytes**
20H -2FH	**Bit Addressable RAM**	**16 Bytes**
1FH	R7	
	REGISTER BANK 3	
18H	R0	
17H	R7	
	REGISTER BANK 2	**32 Bytes**
10H	R0	
0FH	R7	
	REGISTER BANK 1	
08H	R0	
07H	R7	
	REGISTER BANK 0	
00H	R0	

Figure 4.1.2 RAM Allocation in 8051

[Source: "The 8051Microcontroller and Embedded Systems: Using Assembly and C" by Mohamed Ali Mazidi, Janice Gillispie Mazidi, Rolin McKinlay]

The lower 32 bytes are divided into 4 separate banks. Each register bank has 8 registers of one byte each. A register bank is selected depending upon two bank select bits in the PSW register as shown in Figure 4.1.2.

- Next 16 bytes are bit addressable. In total, 128bits (16X8) are available in addressable area. Each bit can be accessed and modified by suitable instructions. The bit addresses are from 00H (LSB of the first byte in 20H) to 2FH (MSB of the last byte in 2FH).
- Remaining 80bytes of RAM (30H TO 7FH) are available for general purpose.

INTERNAL ARCHITECTURE OF 8051 MICROCONTROLLER

The Internal architecture is shown in Figure 4.1.4 and the various Registers and units are described below.

Accumulator (Acc):

•Operand register

• Implicit or specified in the instruction

•Has an address in on chip SFR bank

B Register:

Used to store one of the operands for multiplication and division, otherwise, scratch pad considered as a SFR.

Stack Pointer (SP):

8 bit wide register. Incremented before data is stored on to the stack using PUSH or CALL instructions. Stack defined anywhere on the 128 byte RAM.

Data Pointer (DPTR)*:*

*1*6 bit register contains DPH and DPL Pointer to external RAM address. DPH and DPL allotted separate addresses in SFR bank

Port 0 To 3 Latches & Drivers:

Each I/O port allotted a latch and a driver Latches allotted address in SFR. User can communicate via these ports P0, P1, P2, and P3.

Serial Data Buffer:

Internally had TWO independent registers, TRANSMIT buffer (parallel in serial out – PISO) and RECEIVE buffer (serial in parallel out –SIPO) identified by SBUF and allotted an address in SFR.

Program Status Word (PSW):

Set of flags contains status information as detailed below in the Figure 4.1.3.

CY	AC	F0	RS1	RS0	OV	–	P

CY	PSW.7	Carry flag.
AC	PSW.6	Auxiliary carry flag.
F0	PSW.5	Available to the user for general purpose.
RS1	PSW.4	Register Bank selector bit 1.
RS0	PSW.3	Register Bank selector bit 0.
OV	PSW.2	Overflow flag.
–	PSW.1	User-definable bit.
P	PSW.0	Parity flag. Set/cleared by hardware each instuction cycle to indicate an odd/even number of 1 bits in the accumulator.

RS1	RS0	Register Bank	Address
0	0	0	00H - 07H
0	1	1	08H - 0FH
1	0	2	10H - 17H
1	1	3	18H - 1FH

Figure 4.1.3 Bits of PSW Register

[Source: "The 8051Microcontroller and Embedded Systems: Using Assembly and C" by Mohamed Ali Mazidi, Janice Gillispie Mazidi, Rolin McKinlay , pg.no.52]

Timer Registers: for Timer0 (16 bit register – TL0 & TH0) and for Timer1 (16 bit register – TL1 & TH1) four addresses allotted in SFR

Control Registers: Control registers are IP, IE, TMOD, TCON, SCON, and PCON. These registers contain control and status information for interrupts, timers/counters and serial port. Allotted separate address in SFR.

Timing and Control Unit: This unit derives necessary timing and control signals for internal circuit and external system bus.

Oscillator: generates basic timing clock signal using crystal oscillator.

Instruction Register: Decodes the opcode and gives information to timing and control unit.

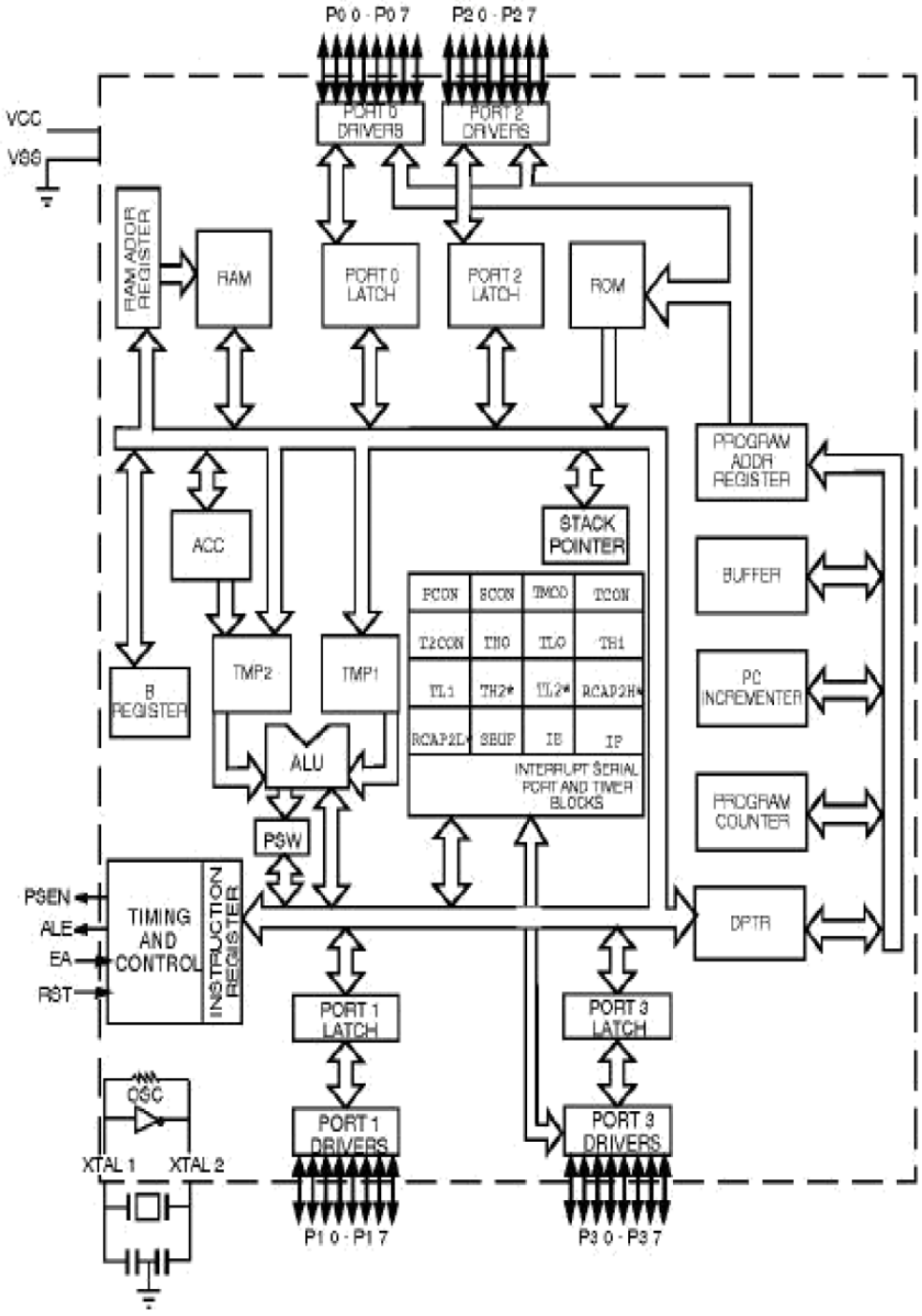

Figure 4.1.4 8051 Architecture Block diagram

[Source: "The 8051Microcontroller and Embedded Systems: Using Assembly and C" by Mohamed Ali Mazidi, Janice Gillispie Mazidi, Rolin McKinlay , pg.no.29]

EPROM & program address Register: provide on chip EPROM and mechanism to address it. All versions don't have EPROM.

Ram & Ram Address Register: provide internal 128 bytes RAM and a mechanism to address internally

ALU: Performs 8 bit arithmetic and logical operations over the operands held by TEMP1 and TEMP 2.User cannot access temporary registers.

SFR Register Bank: set of special function registers address range: 80 H to FF H. Interrupt, serial port and timer units control and perform specific functions under the control of timing and control unit.

8051 PIN CONFIGURATION

The pin diagram of 8051 microcontroller is shown in Figure 4.1.5 and the pin details are described below.

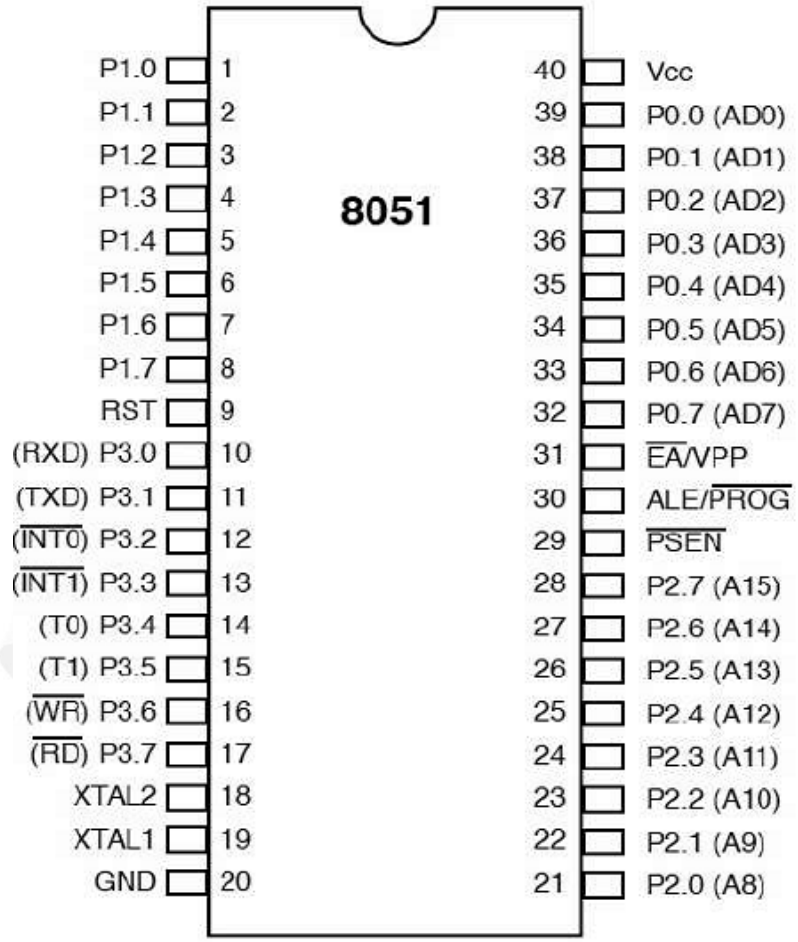

Figure 4.1.5 8051 Pin Configuration

[Source: "The 8051Microcontroller and Embedded Systems: Using Assembly and C" by Mohamed Ali Mazidi, Janice Gillispie Mazidi, Rolin McKinlay , pg.no.94]

Pins 1 to 8 − these pins are known as Port 1. This port doesn't serve any other functions. It is internally pulled up, bi-directional I/O port.

Pin 9 − It is a RESET pin, which is used to reset the microcontroller to its initial values.

Pins 10 to 17 − These pins are known as Port 3. This port serves some alternate functions like interrupts, timer input, control signals, serial communication signals RxD and TxD, etc.

P3 Bit	Function	Pin
P3.0	RxD	10
P3.1	TxD	11
P3.2	$\overline{\text{INT0}}$	12
P3.3	$\overline{\text{INT1}}$	13
P3.4	T0	14
P3.5	T1	15
P3.6	$\overline{\text{WR}}$	16
P3.7	$\overline{\text{RD}}$	17

Figure 4.1.6 Port 3 Alternate Functions

[Source: "The 8051Microcontroller and Embedded Systems: Using Assembly and C" by Mohamed Ali Mazidi, Janice Gillispie Mazidi, Rolin McKinlay , pg.no.97]

Pins 18 & 19 − These pins are used for interfacing an external crystal to get the system clock.

Pin 20 − This pin provides the power supply to the circuit.

Pins 21 to 28 − These pins are known as Port 2. It serves as I/O port. Higher order address bus signals are also multiplexed using this port.

Pin 29 − This is PSEN pin which stands for Program Store Enable. It is used to read a signal from the external program memory.

Pin 30 − This is EA pin which stands for External Access input. It is used to enable/disable the external memory interfacing.

Pin 31 − This is ALE pin which stands for Address Latch Enable. It is used to demultiplex the address-data signal of port.

Pins 32 to 39 − These pins are known as Port 0. It serves as I/O port. Lower order address and data bus signals are multiplexed using this port.

Pin 40 − This pin is used to provide power supply to the circuit.