## 1.8 EMITTER COUPLED LOGIC (ECL)

Emitter-coupled logic is the fastest of all digital logic families. It was invented by Hannon S. Yourke in the year 1956 at IBM. It is also called as current mode logic. The design of ECL circuit consists of transistors and resistors.

By preventing the transistor from entering into saturation, the high-speed operation is achieved in ECL logic family. Very small voltage swing is necessary to switch between the two different voltage levels. This cannot be achieved in transistor-transistor logic, as the transistors enter into saturation mode, while in operation.

Emitter-coupled logic family offers an incredible propagation delay of 1ns. The delay is more reduced in the latest ECL families. In this section, you will learn about the operation of basic emitter coupled logic implemented for inverter circuit and OR/NOR gate.

### Inverter circuit of emitter-coupled logic

The circuit shown below represents the emitter-coupled logic circuit of an inverter. It has two NPN transistors connected in differential single-ended input mode.

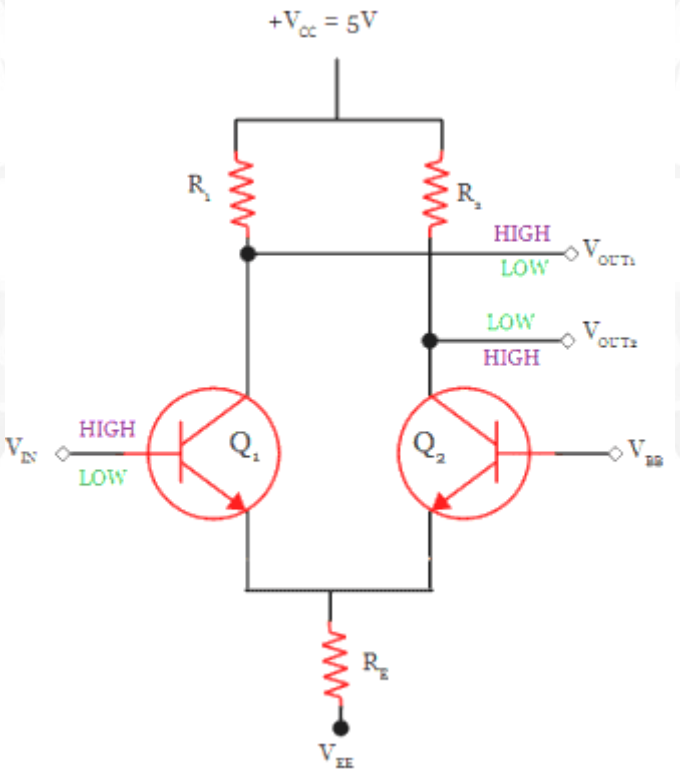


**Figure 1.8.1 Emitter-Coupled Logic**

*[Source: https://www.electrically4u.com/emitter-coupled-logic]*

Both the emitters are connected together with common resistance $R_E$. It is a current limiting resistance, used to prevent the transistor from entering into saturation.

It has two outputs: inverting output($V_{OUT1}$) and non-inverting output($V_{OUT12}$). $V_{IN}$ is the input terminal, where LOW or HIGH input is given.

When the input is HIGH, it will turn ON the transistor $Q_1$ but not saturated and the transistor $Q_2$ is turned OFF. This will pull the output $V_{OUT2}$ to HIGH but due to the drop in resistant $R_1$, the output at terminal $V_{OUT1}$ will be at LOW value.

On the other side, when the input $V_{IN}$ is given LOW value, it will turn OFF the transistor $Q_1$ and the transistor is turned ON. The transistor $Q_2$ will not enter into saturation.

It will make the output at terminal $V_{OUT1}$ to be pulled HIGH value. Due to the drop in resistance $R_2$, the output at terminal $V_{OUT2}$ will have LOW value.

**Two input ECL OR/NOR gate**

The following circuit is the Emitter-coupled logic circuit of the 2-input OR/NOR gate. It is the slight modification of the inverter circuit given above. In this, an additional transistor is used at the input side.

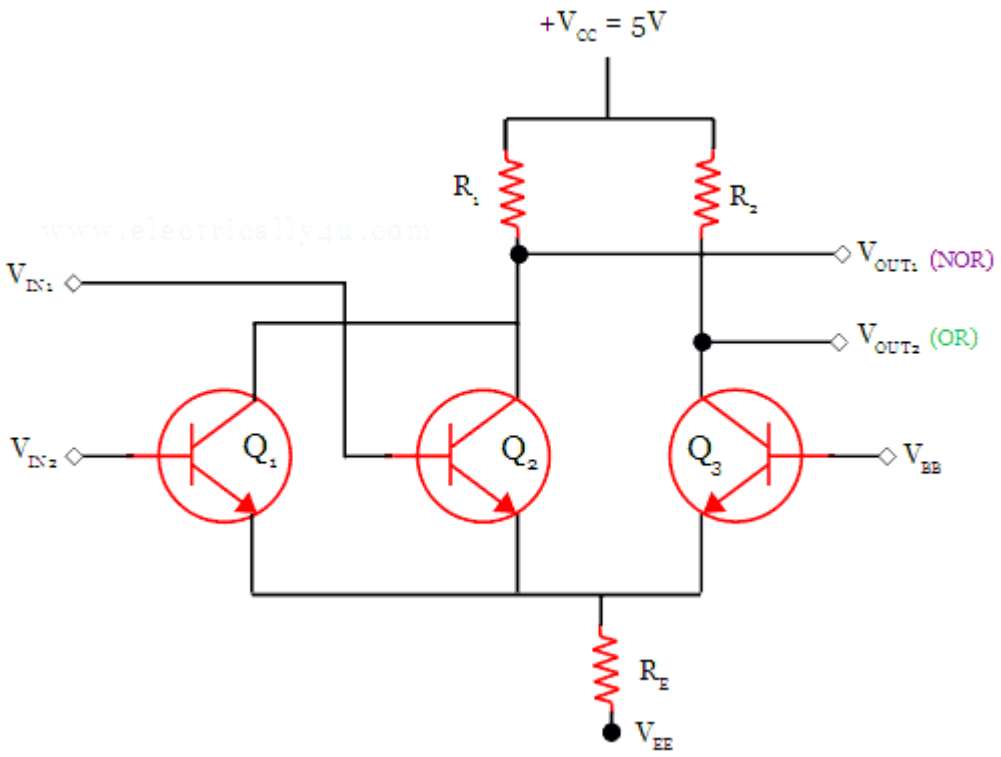


**Figure 1.8.2 Two input ECL OR/NOR gate**

*[Source: https://www.electrically4u.com/emitter-coupled-logic]*

The operation is simple as explained above. If the input at both the transistors $Q_1$ and $Q_2$ are LOW, it will make $V_{OUT1}$ to HIGH value. It corresponds to the NOR gate output. At the same time, transistor $Q_3$ is turned ON, which will make the $V_{OUT2}$ to be HIGH. It corresponds to the OR gate output.

Similarly, if both the input of transistors $Q_1$ and $Q_2$ are HIGH, it will turn on both the transistors. It will drive the output at terminal $V_{OUT1}$ to be LOW. The transistor $Q_3$ is turned OFF during this operation. It will drive the output at terminal $V_{OUT2}$ to be HIGH. The truth table for OR/NOR gate is shown below.

| Inputs | | OR | NOR |
|---|---|---|---|
| A | B | Y | Y |
| 0 | 0 | 0 | 1 |
| 0 | 1 | 1 | 0 |
| 1 | 0 | 1 | 0 |
| 1 | 1 | 1 | 0 |

Advantages

- High-speed operation is possible and so the fastest logic family.
- Since transistors are not allowed to enter into saturation, which reduces the storage delay.
- Fan-out capability is high.

Apart from the advantages, it also has its own disadvantage. For the fast switching of transistors, the low and high logic levels are kept close. It reduces the noise margin. Since transistors are not allowed to enter into saturation, the power consumption is more.