UNIT II

MICROPROCESSOR AND MICROCONTROLLER

- Bus Structure
- Pin Configuration of 8085
- Addressing Modes
- Instruction Sets

2.2.1 8085 Bus Structure

i. Address bus :

- The address bus is a group of 16 lines generally identified as A_0 to A_{15}.
- The address bus is unidirectional : bits flow in one direction-from the MPU to peripheral devices.
- The MPU uses the address bus to perform the first function : identifying a peripheral or a memory location.

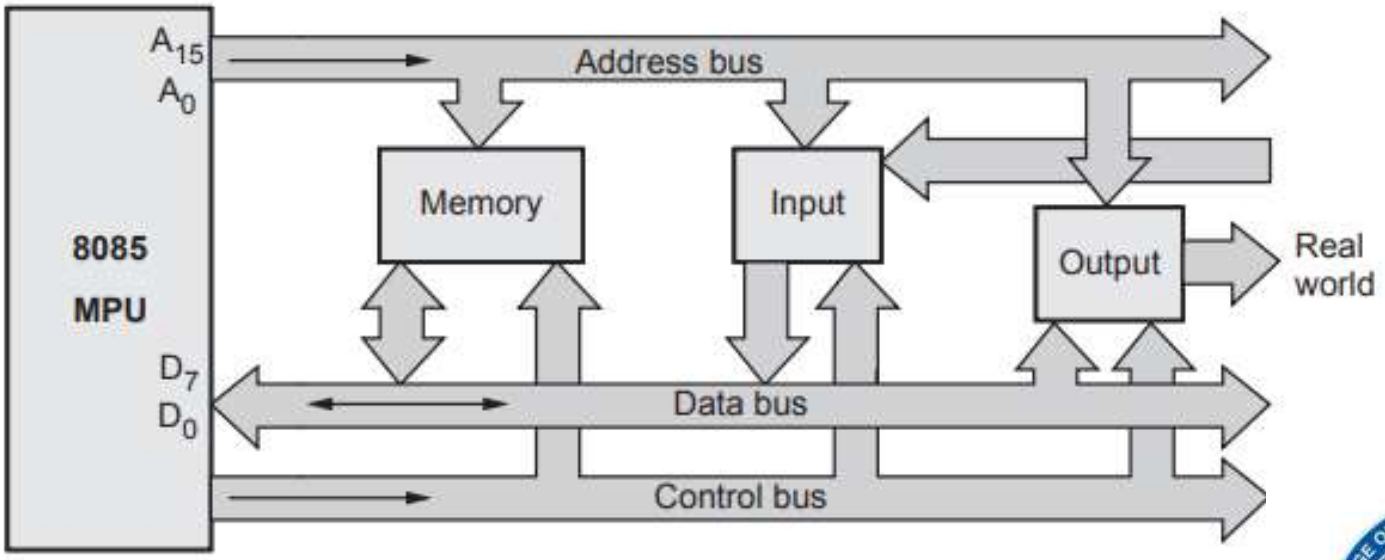


Fig. 2.2.2

ii. Data bus :

The data bus is a group of eight lines used for data flow.

- These lines are bi-directional - data flow in both directions between the MPU and memory and peripheral devices.
- The MPU uses the data bus to perform the second function: transferring binary information.
- The eight data lines enable the MPU to manipulate 8 - bit data ranging from 00 to FF (28 = 256 numbers).
- The largest number that can appear on the data bus is 11111111.

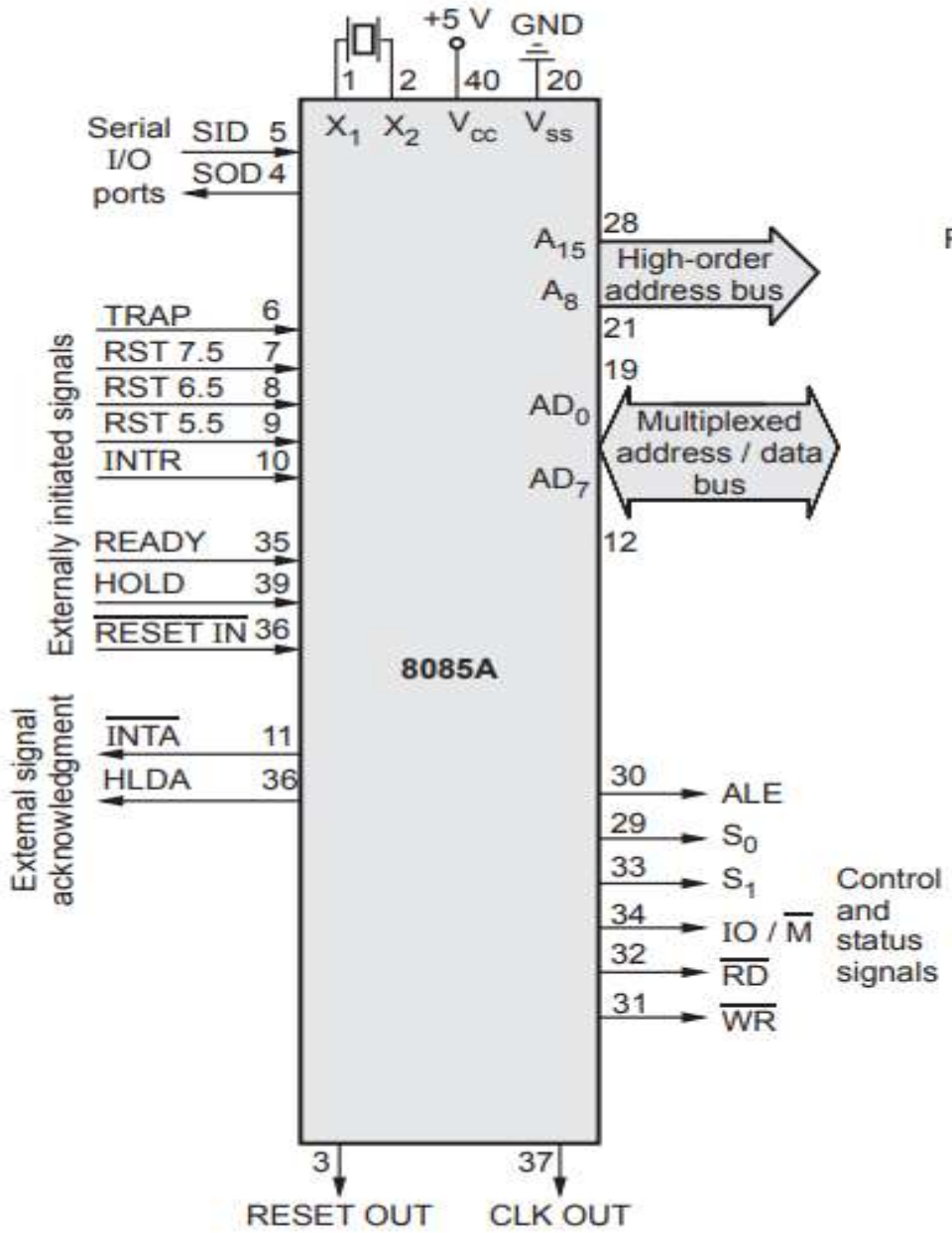
iii. Control bus :

- The control bus carries synchronization signals and providing timing signals.
- The MPU generates specific control signals for every operation it performs. These signals are used to identify a device type with which the MPU wants to communicate.

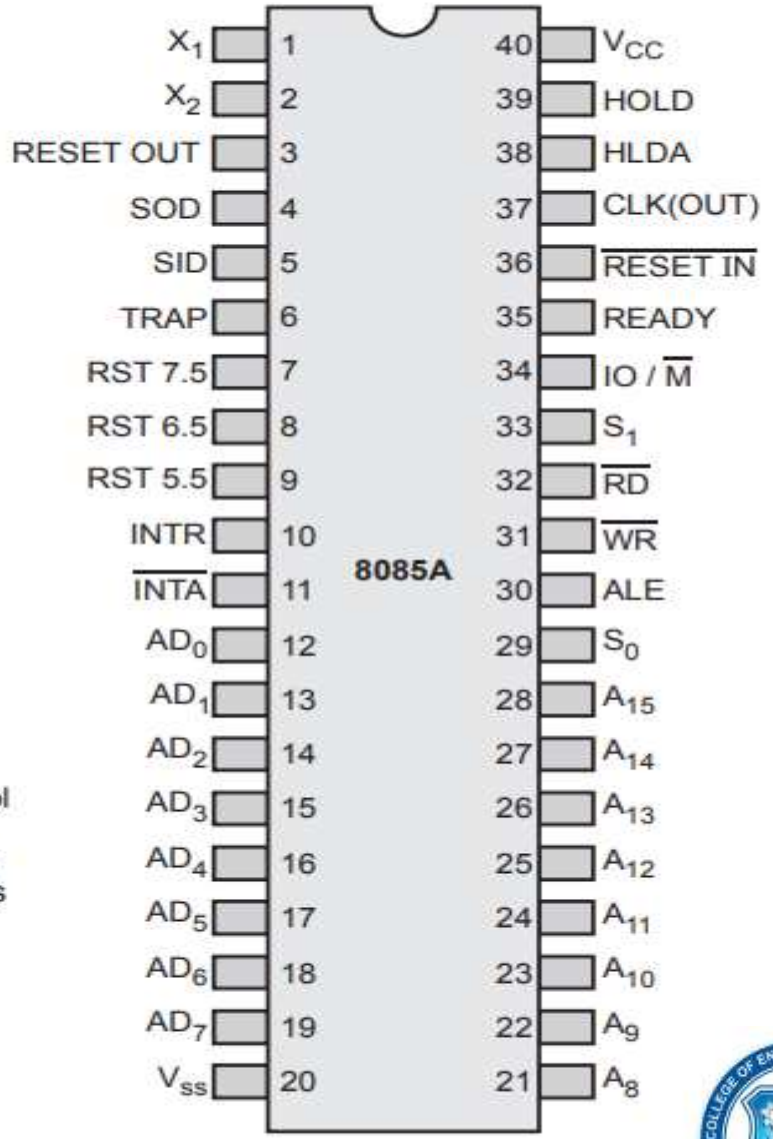
2.3 Pin Diagram and Pin Description of 8085

- 8085 is a 40 pin IC, DIP package.
- The signals from the pins can be grouped as follows

1. Power supply and clock signals
2. Address bus
3. Data bus
4. Control and status signals
5. Interrupts and externally initiated signals
6. Serial I/O ports



(a) Functional pin diagram



(b) Pin configuration

1. Power supply and clock frequency signals

- Vcc + 5 volt power supply
- Vss Ground
- X_1, X_2 : Crystal or R/C network or LC network connections to set the frequency of internal clock generator.
- The frequency is internally divided by two. Since the basic operating timing frequency is 3 MHz, a 6 MHz crystal is connected externally.
- CLK (output) - Clock output is used as the system clock for peripheral and devices interfaced with the microprocessor.

2. Address Bus :

- A_8 - A_{15} (output; 3 - state)
- It carries the most significant 8 bits of the memory address or the 8 bits of the I/O address.

3. Multiplexed Address / Data Bus :

- AD_0 - AD_7 (input/output; 3-state) .
- These multiplexed set of lines used to carry the lower order 8 bit address as well as data bus.
- During the opcode fetch operation, in the first clock cycle, the lines deliver the lower order address A_0 - A_7.
- In the subsequent IO / memory, read / write clock cycle the lines are used as data bus.
- The CPU may read or write out data through these lines.

4. Control and Status signals :

- ALE (output) - Address Latch Enable.
- This signal helps to capture the lower order address presented on the multiplexed address / data bus.
- RD (output 3 - state, active low) - Read memory or IO device.
- This indicates that the selected memory location or I/O device is to be read and that the data bus is ready for accepting data from the memory or I/O device.
- WR (output 3 - state, active low) - Write memory or IO device.
- This indicates that the data on the data bus is to be written into the selected memory location or I/O device.
- IO/M (output) - Select memory or an IO device.

- This status signal indicates that the read / write operation relates to whether the memory or I/O device.
- It goes high to indicate an I/O operation.
- It goes low for memory operations.

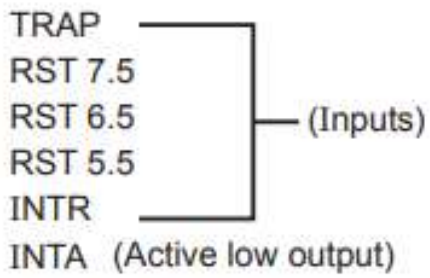
5. Status Signals :

It is used to know the type of current operation of the microprocessor.

IO/M (Active low)	S_1	S_2	Data bus status(output)
0	0	0	Halt
0	0	1	Memory WRITE
0	1	0	Memory READ
1	0	1	IO WRITE
1	1	0	IO READ
0	1	1	Opcode fetch
1	1	1	Interrupt acknowledge

6. Interrupts and externally initiated operations :

- They are the signals initiated by an external device to request the microprocessor to do a particular task or work.
- There are five hardware interrupts called,



- On receipt of an interrupt, the microprocessor acknowledges the interrupt by the active low INTA (Interrupt Acknowledge) signal.

Reset In (input, active low)

- This signal is used to reset the microprocessor.
- The program counter inside the microprocessor is set to zero.
- The buses are tri - stated.

Reset Out (output)

- It indicates CPU is being reset.
- Used to reset all the connected devices when the microprocessor is reset

7. Direct Memory Access (DMA) :

Tri state devices :

- 3 output states are high and low states and additionally a high impedance state.
- When enable E is high the gate is enabled and the output Q can be 1 or 0 (if A is 0, Q is 1, otherwise Q is 0). However, when E is low the gate is disabled and the output Q enters into a high impedance state.

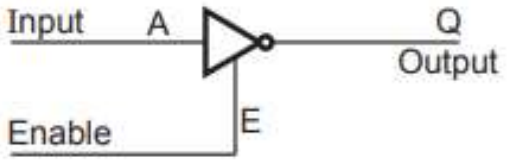


Fig. 2.3.2

E	A	Q	State
1 (high)	0	1	High
1	1	0	Low
0 (low)	0	0	High impedance
0	1	0	High impedance

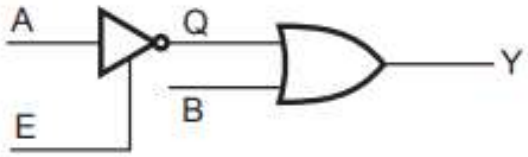


Fig. 2.3.3

For both high and low states, the output Q draws a current from the input of the OR gate.

8. Single Bit Serial I/O ports :

- SID (input) - Serial input data line
- SOD (output) - Serial output data line
- These signals are used for serial communication.

2.4 8085 Addressing Modes

☞ [AU : Dec.-2016, 8 Marks]

- The instructions MOV B, A or MVI A, 82H are to copy data from a source into a destination.
- In these instructions the source can be a register, an input port, or an 8-bit number (00H to FFH).
- Similarly, a destination can be a register or an output port.
- The sources and destination are operands.
- The various formats for specifying operands are called the Addressing Modes.
- For 8085, they are :
  1. Immediate addressing.
  2. Register addressing.
  3. Direct addressing.
  4. Indirect addressing.

1. Immediate addressing

- Data is present in the instruction. Load the immediate data to the destination provided.

Example : MVI R, data

2. Register addressing

- Data is provided through the registers.

Example : MOV Rd, Rs

3. Direct addressing

- Used to accept data from outside devices to store in the accumulator or send the data stored in the accumulator to the outside device.
- Accept the data from the port 00H and store them into the accumulator or send the data from the accumulator to the port 01H.

Example : IN 00H or OUT 01H

4. Indirect Addressing

- This means that the Effective Address is calculated by the processor.
- And the contents of the address (and the one following) is used to form a second address.
- The second address is where the data is stored.
- Note that this requires several memory accesses; two accesses to retrieve the 16-bit address and a further access (or accesses) to retrieve the data which is to be loaded into the register.

2.5 Instruction Set of 8085

☞ [AU : Dec.-2016, 8 Marks]

- An instruction is a binary pattern designed inside a microprocessor to perform a specific function.
- The entire group of instructions that a microprocessor supports is called **Instruction Set.**
- 8085 has **246** instructions.
- Each instruction is represented by an 8-bit binary value.
- These 8-bits of binary value is called **Op - Code** or **Instruction Byte.**

2.5.1 Classification of Instruction Set

1. Data Transfer Instruction
2. Arithmetic Instructions
3. Logical Instructions
4. Branching Instructions
5. Control Instructions

Thank You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