4.1 Asynchronous Sequential Circuits

Asynchronous sequential circuits do not use clock signals as synchronous circuits do. Instead, the circuit is driven by the pulses of the inputs which means the state of the circuit changes when the inputs change. Also, they don't use clock pulses. The change of internal state occurs when there is a change in the input variable. Their memory elements are either un-clocked flip-flops or time-delay elements. They are similar to combinational circuits with feedback.

Advantages –

- No clock signal, hence no waiting for a clock pulse to begin processing inputs, therefore fast. Their speed is faster and theoretically limited only by propagation delays of the logic gates.
- Robust handling. Higher performance function units, which provide average-case completion rather than worst-case completion. **Lower power consumption** because no transistor transitions when it is not performing useful computation. The absence of clock drivers reduces power consumption. Less severe electromagnetic interference (EMI).
- More tolerant to process variations and external voltage fluctuations. Achieve high performance while gracefully handling variable input and output rates and mismatched pipeline stage delays. Freedom from difficulties of distributing a high-fan-out, timing-sensitive clock signal. Better modularity.
- **Less assumptions** about the manufacturing process. Circuit speed adapts to changing temperature and voltage conditions. Immunity to transistor-to-transistor variability in the manufacturing process, which is one of the most serious problems faced by the semiconductor industry

Disadvantages –

- Some asynchronous circuits may require extra power for certain operations.
- More **difficult to design** and subject to problems like sensitivity to the relative arrival times of inputs at gates. If transitions on two inputs arrive at almost the same time, the circuit can go into the wrong state depending on slight differences in the propagation delays of the gates which are known as **race condition**.

- The number of circuit elements (transistors) maybe double that of synchronous circuits. Fewer people are trained in this style compared to synchronous design. Difficult to test and debug. Their **output** is **uncertain**.
- The performance of asynchronous circuits may be reduced in architectures that have a complex data path. Lack of dedicated, asynchronous design-focused commercial EDA tools.