**Domino gates**

The various drawbacks can be overcome by the following logics:

- Domino logic
- Dual-rail Domino logic
- Keepers
- Multiple output Domino logic
- NP and Zipper Domino

**a. Domino Logic**

The monotonicity problem can be solved by placing a static CMOS inverter between dynamic gates, as shown in Figure 2.4.1 (a). This converts the monotonically falling output into a monotonically rising signal suitable for the next gate, as shown in Figure 2.4.1 (b). The dynamic-static pair together is called a domino gate because Precharge resembles setting up a chain of dominos and evaluation causes the gates to fire like dominos tipping over, each triggering the next. A single clock can be used to Precharge and evaluate all the logic gates within the chain. The dynamic output is monotonically falling during evaluation, so the static inverter output is monotonically rising. Therefore, the static inverter is usually a HI-skew gate to favor this rising output. Observe that Precharge occurs in parallel, but evaluation occurs sequentially. The symbols for the dynamic NAND, HI-skew inverter, and domino AND are shown in Figure 2.4.1(c).

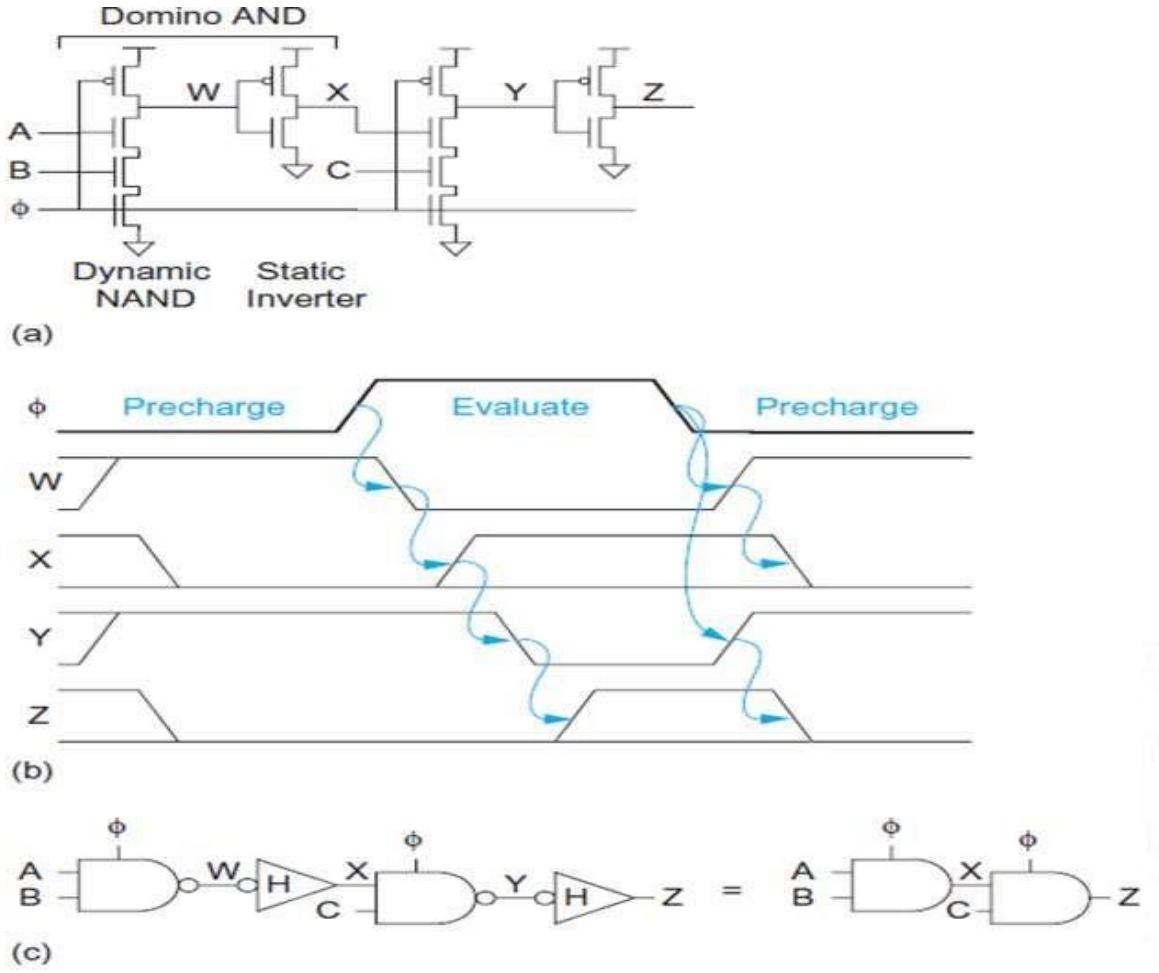


**Figure 2.4.1: Domino Gates**

[Source: Neil H.E. Weste, David Money Harris —CMOS VLSI Design]

## b. Dual-Rail Domino Logic

Dual-rail domino gates encode each signal with a pair of wires. The input and output signal pairs are denoted with _h and _l, respectively. summarizes the encoding. The _h wire is asserted to indicate that the output of the gate is "high" or 1. The wire is asserted to indicate that the output of the gate is "low" or 0. When the gate is Precharge, neither _h nor _l is asserted. The pair of lines should never be both asserted simultaneously during correct operation. Dual-rail domino gates accept both true and complementary inputs and compute both true and complementary outputs, as shown in Figure 2.4.2 (a). Observe that this is identical to static CVSL circuits from Figure 2.4.2except that the cross-coupled pMOS

transistors are instead connected to the Precharge clock. Therefore, dual-rail domino can be viewed as a dynamic form of CVSL, sometimes called DCVS. Figure 2.4.2 (b) shows a dual-rail AND/NAND gate and Figure 2.4.2(c) shows a dual-rail XOR/XNOR gate.

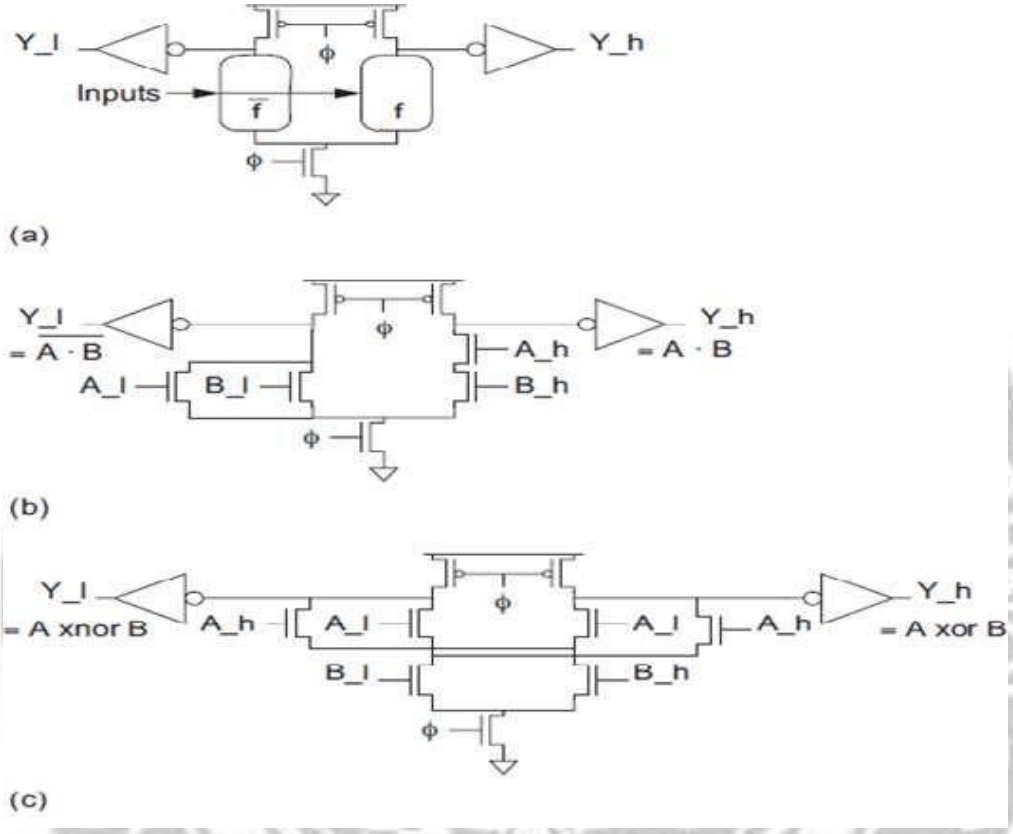


**Figure 2.4.2: Domino Rail Domino Gates**

[Source: Neil H.E. Weste, David Money Harris —CMOS VLSI Design]

Dual-rail structures also neither lose the efficiency of wide dynamic NOR gates because they require complementary tall dynamic NAND stacks. Dual-rail domino signals not only the result of a computation but also indicates when the computation is done. Before computation completes, both rails are Precharge. When the computation completes, one rail will be asserted. A NAND gate can be used for completion detection, as shown in Figure 2.4.3. Coupling can be reduced in dual-rail signal busses by inter digitating the bits of the bus, as shown in Figure 9.32. Each wire will never see more than one aggressor switching at a time because only one of the two rails switches in each cycle.

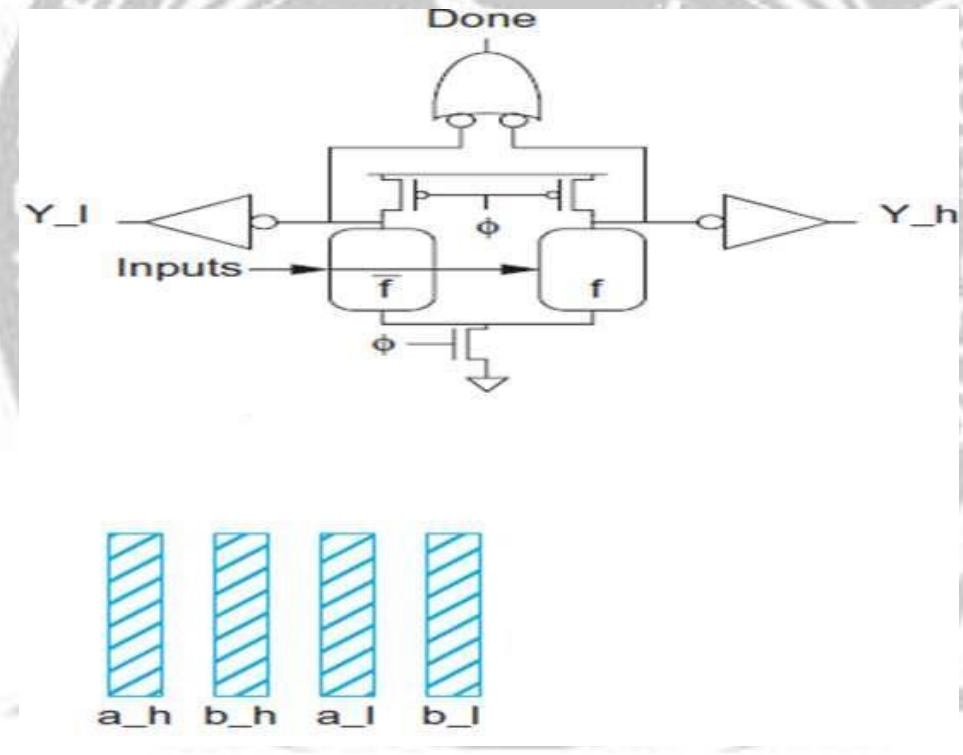


**Figure 2.4.3: Domino Rail Domino Gates with completion Reduction**

[Source: Neil H.E. Weste, David Money Harris —CMOS VLSI Design]

## C.Keepers

Dynamic circuits also suffer from charge leakage on the dynamic node. If a dynamic

node is precharged high and then left floating, the voltage on the dynamic node will drift over time due to sub threshold, gate, and junction leakage. The time constants tend to be in the millisecond to nanosecond range, depending on process and temperature. This problem is analogous to leakage in dynamic RAMs. Moreover, dynamic circuits have poor input noise margins. If the input rises above Vt while the gate is in evaluation, the input transistors will turn on weakly and can incorrectly discharge the output. Both leakage and noise margin problems can be addressed by adding a keeper circuit. Figure 2.4.4 shows a conventional keeper on a domino buffer. The keeper is a weak transistor that holds, or staticizes, the output at the correct level when it would otherwise float. When the dynamic node X is high, the output Y is low and the keeper is ON to pre- vent X from floating. When X falls, the keeper initially opposes the transition so it must be much weaker than the pull down network. Eventually Y rises, turning the keeper OFF and avoiding static power dissipation.

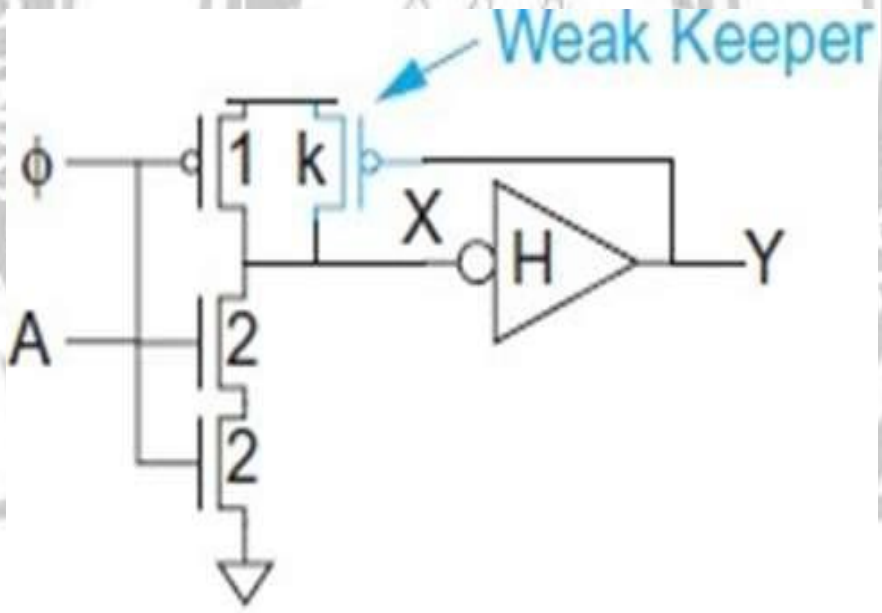


**Figure 2.4.4: Conventional Keeper**

[Source: Neil H.E. Weste, David Money Harris —CMOS VLSI Design]

## c. Multiple-Output Domino Logic (MODL)

It is often necessary to compute multiple functions where one is a subfunction of another or shares a subfunction. Multiple-output domino logic (MODL) [Hwang89, Wang97] saves area by combining all of the computations into a multiple-output gate. A popular application is in addition, where the carry-out ci of each bit of a 4-bit block must be computed, as discussed in Section 11.2.2.2. Each bit position i in the block can either propagate the carry (pi) or generate a carry (gi). The carry-out logic is

$$c_1 = g_1 + p_1 c_0$$
$$c_2 = g_2 + p_2(g_1 + p_1 c_0)$$
$$c_3 = g_3 + p_3(g_2 + p_2(g_1 + p_1 c_0))$$
$$c_4 = g_4 + p_4(g_3 + p_3(g_2 + p_2(g_1 + p_1 c_0)))$$

This can be implemented in four compound AOI gates, as shown in Figure

2.4.5(a). Notice that each output is a function of the less significant outputs. The more compact MODL design shown in Figure 2.4.5 (b) is often called a Manchester carry chain.

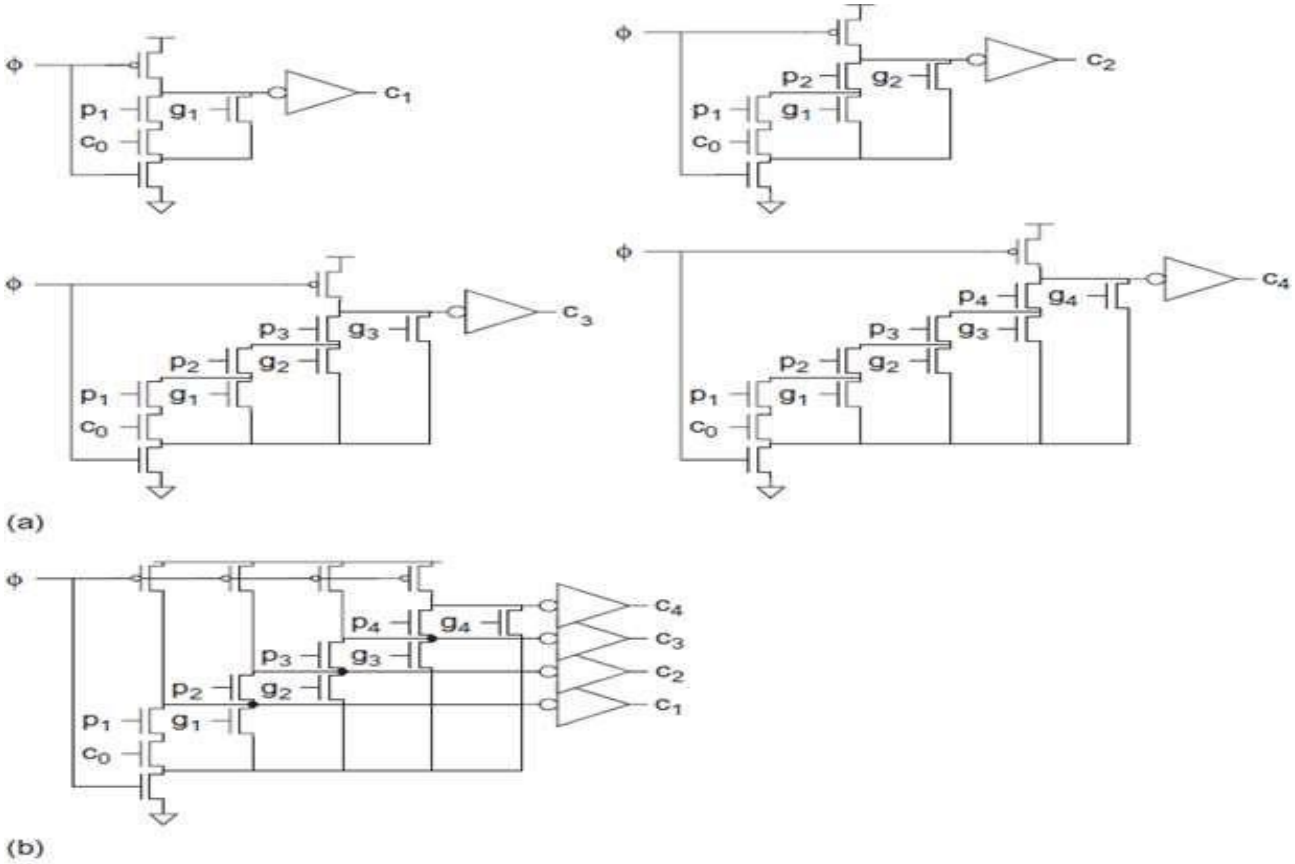


**Figure 2.4.5: Conventional and MODL Carry Chains**

[Source: Neil H.E. Weste, David Money Harris —CMOS VLSI Design]

## d. NP and Zipper Domino

Another variation on domino is shown in Figure 9.46(a). The HI-skew inverting static gates are replaced with predischarged dynamic gates using pMOS logic. For example, a footed dynamic p-logic NAND gate is shown in Figure 9.46(b). When K is 0, the first and third stages precharge high while the second stage pre- discharges low. When K rises, all the stages evaluate. Domino connections are possible, as shown in Figure 9.46(c). The design style is called NP Domino or NORA Domino.

**Disadvantages**

- Logical effort is the worst

- Susceptible to noise

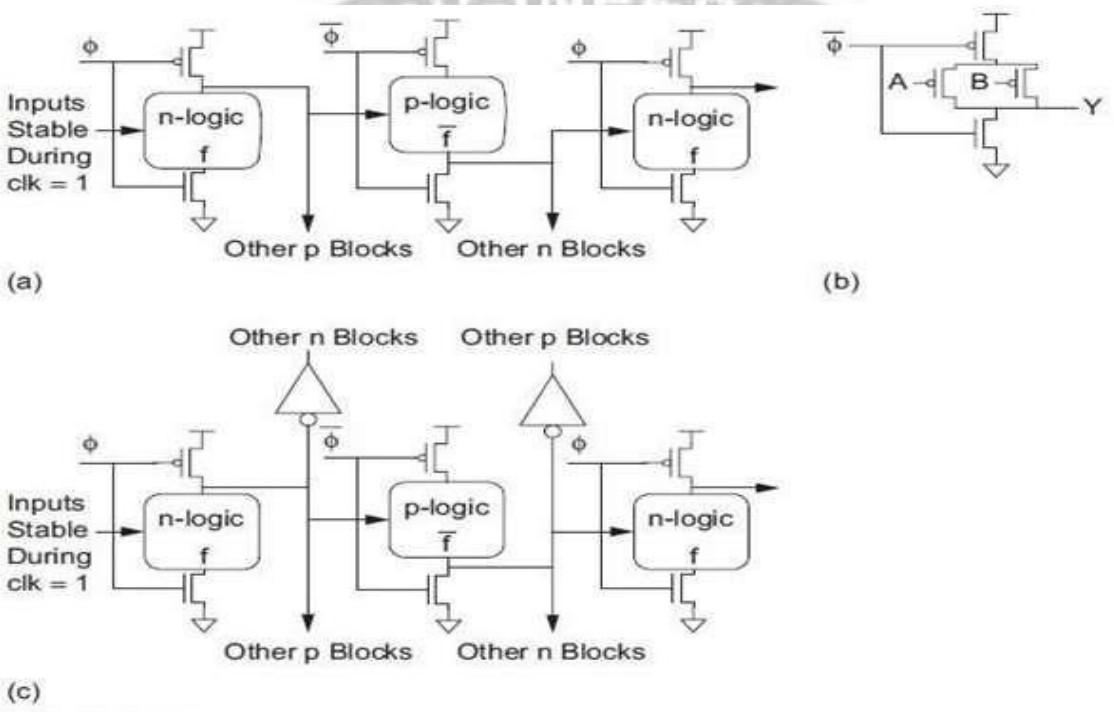


**Figure 2.4.6: NP Domino**

[Source: Neil H.E. Weste, David Money Harris —CMOS VLSI Design]

**Pass Transistor Circuits:**

- In pass transistor circuits, inputs are also applied to the source/drain diffusion terminals.
- These circuits build switches using either n MOS pass transistor or parallel pairs of nM\OS and p MOS transistors called transmission gates.
- For example pass transistors are essential to the design of efficient 6 transistor static RAM cells used in most modern systems.
- Full address and other circuits rich in XOR s also can b efficiently constructed with pass transistors.

## CMOS with Transmission Gates:

- Structures such as tristates, latches and multiplexers are often drawn as transmission gates in conjection with simple static CMOS Logic.
- The logic levels on the output are no better than those on the input so a cae of such circuits may accumulate Noise.
- To buffer the output and restore levels a static CMOS output inverter can be added.
- At first CMOS with transmission gates might appear to offer an entirely new range of circuits. The examination shows that the topology is almost identical to static CMOS.
- If multiple stages of logic are cae they can be viewed as alternating transmission gates an inverters.

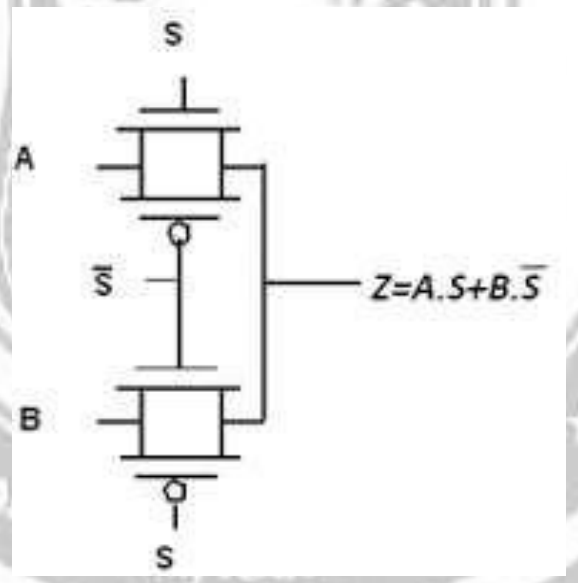


**Figure 2.4.7: Transmission Gates**

[Source: Neil H.E. Weste, David Money Harris —CMOS VLSI Design]

- The above figure redraws the multiplexes to include the inverters from the previous that drive the diffusion input but to exclude in output inverter.
- The intermediate modes in the pull up and pull-down networks are shorted together as N1 and N2.

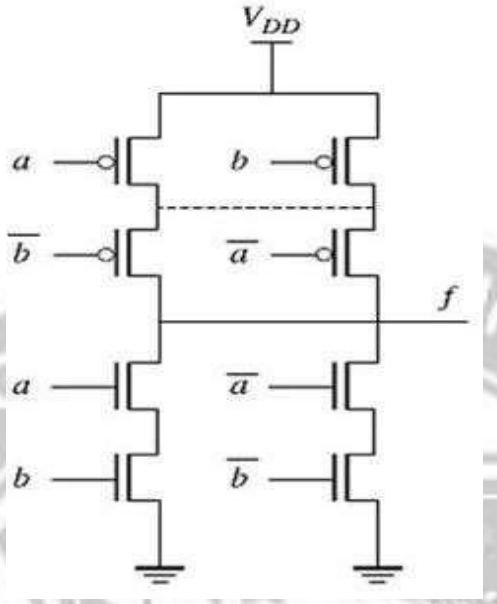


**Figure 2.4.7: CMOS Implementation**

[Source: Neil H.E. Weste, David Money Harris ―CMOS VLSI Design]

- The shorting of the intermediate nodes has two effects on delay.
- Since the output is pulled up or down through the parallel combination of both pass transistor rather than through a single transistor. The effective resistance will be decreased.
- But the effective capacitance increases slightly because of extra diffusion and wire capacitance required for this shorting.
- There are several factors that favor the static CMOS representation over CMOS with transmission gates.
- It the inverter is on the output rather than the input; the delay of the gate depends on what is driving the input as well as the capacitance driver by the output.
- The second drawback is that diffuse inputs to tristate invertors are susceptible to noise that may incorrectly turn on the inverter.
- Finally the contacts slightly increases are and their capacitance increases power consumption.
- The logical effort of circuits involving transmission gates is computed by drawing stage that begin at gate inputs rather than diffusion inputs.

**Complementary pass Transistor Logic(CPL):**

- CVSI is slow because one side of the gate pulls down, and then the cross coupled PMOs transistor pulls the other side up.
- The size of the cross coupled device is an inherent compromise between a large transistor that fights the pull down excessively and a small transistor that is slow pulling up.
- CPL resolves this problem by making on half of the gate pull up while the other half pulls down.
- In the CPL multiplexer. If a path consists of a cae of CPL gates, the inverters can be viewed equally well as being on the output of one stage or the input of the nest stage.
- If we redraws the mux to include the inverters from the previous stage that drives the diffusion input, but to exclude the output inverters.
- When the gate switches, one side pulls down well through its n MOS transistor.
- The other side pulls up.
- CPL can be constructed without cross coupled PMOS transistors, but the outputs would only to VDD-Vt.
- Adding weak cross- coupled devices helps bring the rising output to the supply rail while only slightly slowing the falling output.