UNIT III FIELD EFFECT TRANSISTORS

3.1 JUNCTION FIELD EFFECT TRANSISTOR (JFET)

There are two basic configurations of junction field effect transistor, the N-channel JFET and the P-channel JFET. The N-channel JFET's channel is doped with donor impurities meaning that the flow of current through the channel is negative (hence the term N-channel) in the form of electrons.

Likewise, the P-channel JFET's channel is doped with acceptor impurities meaning that the flow of current through the channel is positive (hence the term P-channel) in the form of holes. N-channel JFET's have a greater channel conductivity (lower resistance) than their equivalent P-channel types, since electrons have a higher mobility through a conductor compared to holes. This makes the N-channel JFET's a more efficient conductor compared to their P-channel counterparts.

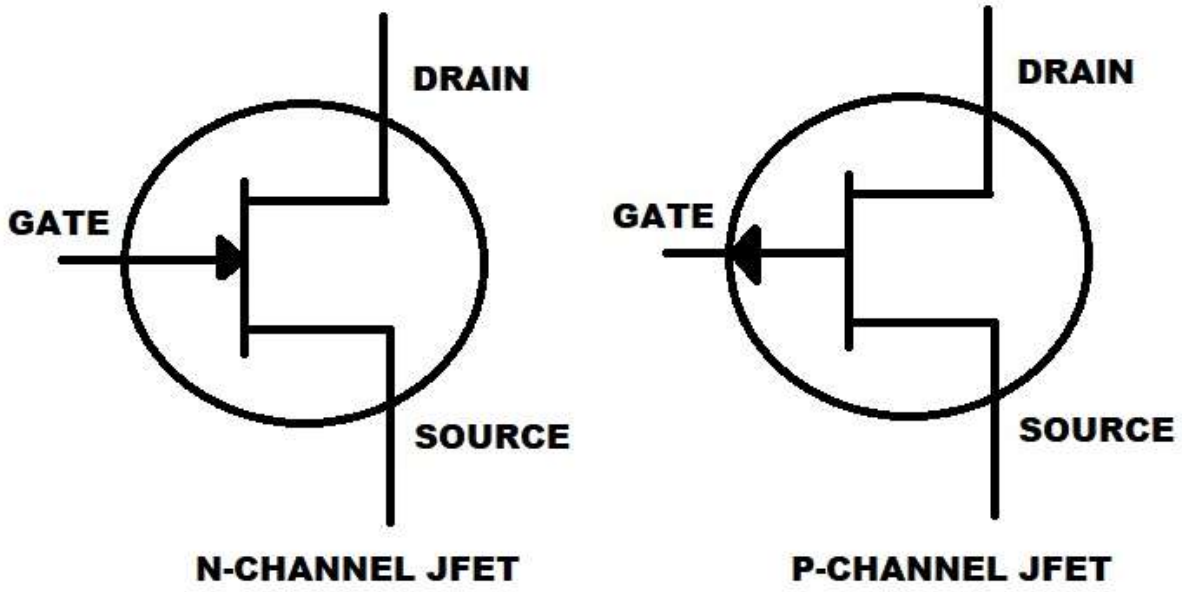

Fig:3.1.1 Symbol of N-Channel and P-Channel JFET

There are two ohmic electrical connections at either end of the channel called the Drain and the Source. But within this channel there is a third electrical connection which is called the Gate terminal and this can also be a P-type or N-type material forming a PN-junction with the main channel.

Construction

The semiconductor "channel" of the Junction Field Effect Transistor is a resistive path through which a voltage VDS causes a current ID to flow and as such the junction

field effect transistor can conduct current equally well in either direction. As the channel is resistive in nature, a voltage gradient is thus formed down the length of the channel with this voltage becoming less positive as go from the Drain terminal to the Source terminal.

The result is that the PN-junction therefore has a high reverse bias at the Drain terminal and a lower reverse bias at the Source terminal. This bias causes a "depletion layer" to be formed within the channel and whose width increases with the bias.

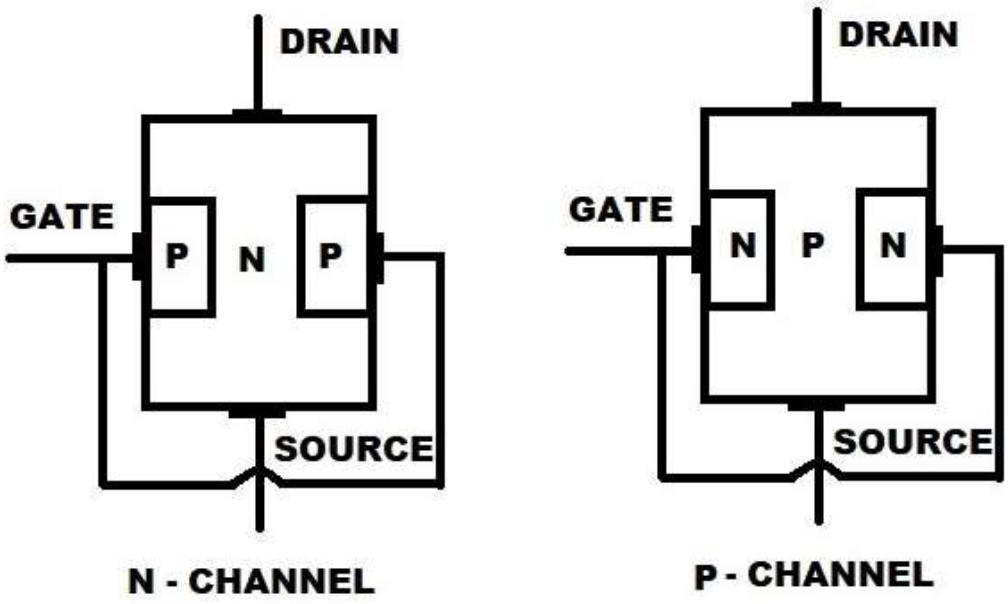

Fig:3.1.2 Construction of N-Channel and P-Channel JFET

The magnitude of the current flowing through the channel between the Drain and the Source terminals is controlled by a voltage applied to the Gate terminal, which is a reverse-biased. In an N-channel JFET this Gate voltage is negative while for a P-channel JFET the Gate voltage is positive.

The main difference between the JFET and a BJT device is that when the JFET junction is reverse-biased the Gate current is practically zero, whereas the Base current of the BJT is always some value greater than zero.

Biasing of N-channel JFET

The cross sectional diagram above shows an N-type semiconductor channel with a P-type region called the Gate diffused into the N-type channel forming a reverse biased PN-junction and it is this junction which forms the depletion region around the Gate area

when no external voltages are applied. JFETs are therefore known as depletion mode devices.

This depletion region produces a potential gradient which is of varying thickness around the PN-junction and restrict the current flow through the channel by reducing its effective width and thus increasing the overall resistance of the channel itself.

The most-depleted portion of the depletion region is in between the Gate and the Drain, while the least-depleted area is between the Gate and the Source. Then the JFET's channel conducts with zero bias voltage applied (ie, the depletion region has near zero width).

With no external Gate voltage (VG = 0), and a small voltage (VDS) applied between the Drain and the Source, maximum saturation current (IDSS) will flow through the channel from the Drain to the Source restricted only by the small depletion region around the junctions.

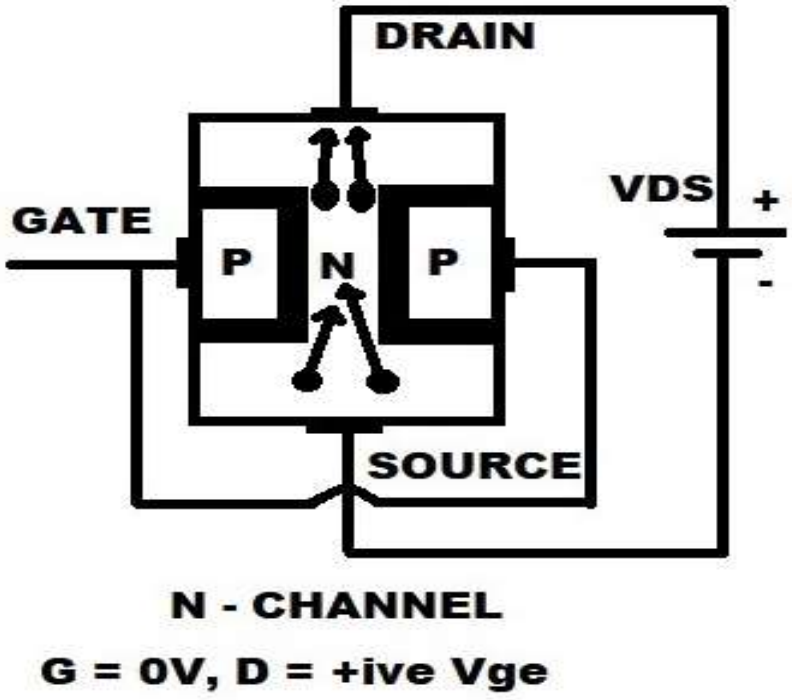

Fig:3.1.3 Working of N-Channel JFET (Gate = 0V, Drain = +ive Vge)

If a small negative voltage (-VGS) is now applied to the Gate the size of the depletion region begins to increase reducing the overall effective area of the channel and thus reducing the current flowing through it, a sort of "squeezing" effect takes place. So

by applying a reverse bias voltage increases the width of the depletion region which in turn reduces the conduction of the channel.

Since the PN-junction is reverse biased, little current will flow into the gate connection. As the Gate voltage (-VGS) is made more negative, the width of the channel decreases until no more current flows between the Drain and the Source and the FET is said to be “pinched-off” (similar to the cut-off region for a BJT). The voltage at which the channel closes is called the “pinch-off voltage”, (VP).

JFET Channel Pinched-off

In this pinch-off region the Gate voltage, VGS controls the channel current and VDS has little or no effect.

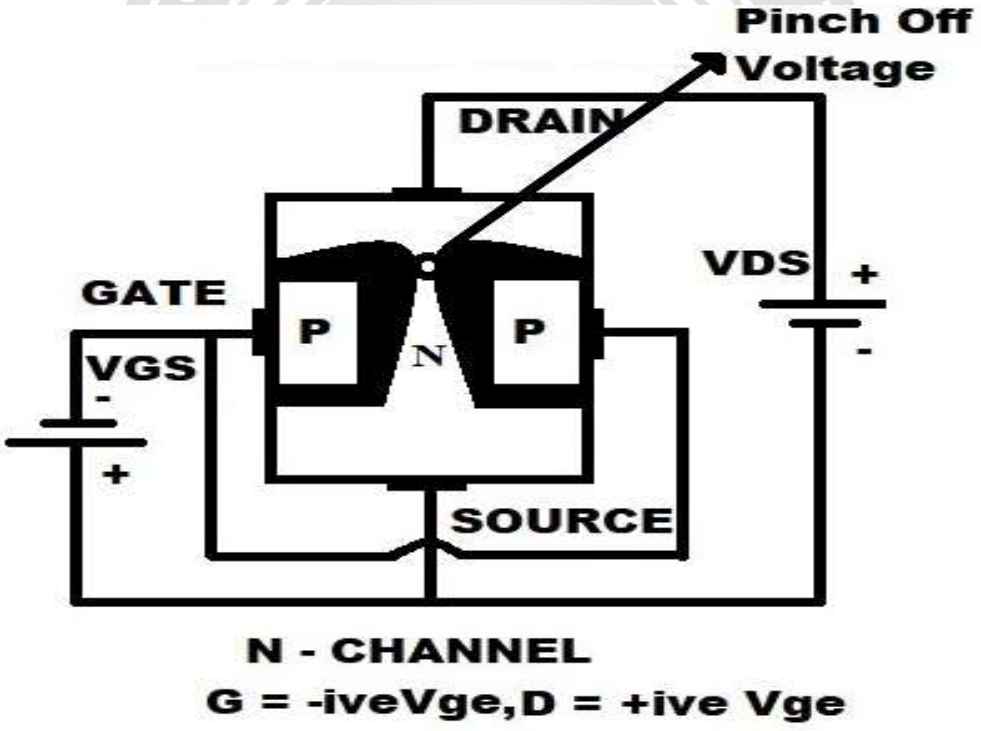

Fig:3.1.4 Working of N-Channel JFET (Gate = -ive Vge, Drain = +ive Vge)

The result is that the FET acts more like a voltage controlled resistor which has zero resistance when VGS = 0 and maximum “ON” resistance (RDS) when the Gate voltage is very negative. Under normal operating conditions, the JFET gate is always negatively biased relative to the source.

It is essential that the Gate voltage is never positive since if it is all the channel current will flow to the Gate and not to the Source, the result is damage to the JFET. Then to close the channel:

- No Gate Voltage (VGS) and VDS is increased from zero.
- No VDS and Gate control is decreased negatively from zero.
- VDS and VGS varying.

The P-channel Junction Field Effect Transistor operates exactly the same as the N-channel above, with the following exceptions: 1). Channel current is positive due to holes, 2). The polarity of the biasing voltage needs to be reversed.

Drain Characteristics

The drain characteristics of an N-channel JFET with the gate short-circuited to the source.

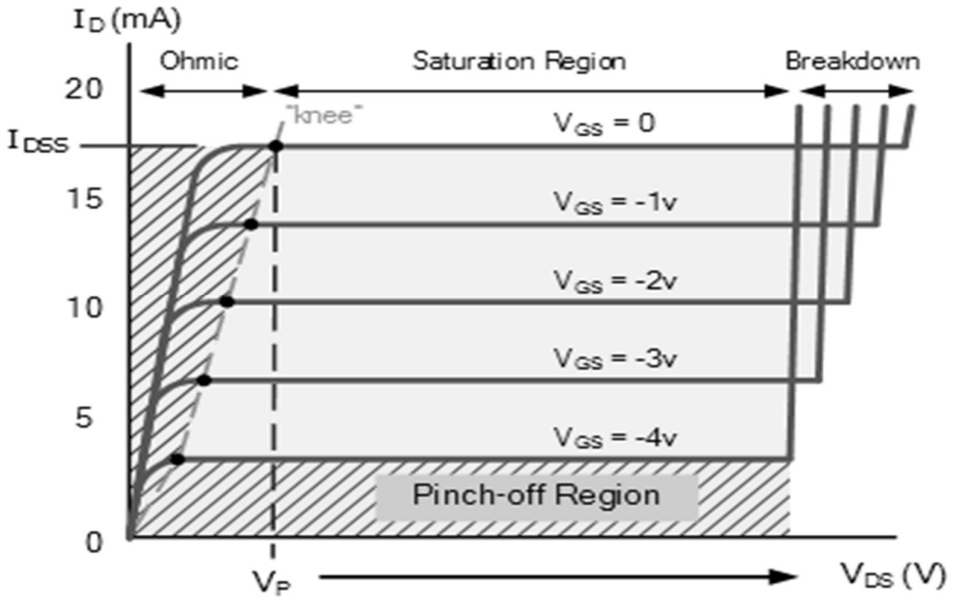

Fig:3.1.5 Drain Characteristics of N-Channel JFET

The voltage VGS applied to the Gate controls the current flowing between the Drain and the Source terminals. VGS refers to the voltage applied between the Gate and the Source while VDS refers to the voltage applied between the Drain and the Source.

Because a Junction Field Effect Transistor is a voltage controlled device, "NO current flows into the gate!" then the Source current (IS) flowing out of the device equals the Drain current flowing into it and therefore (ID = IS).

The characteristics curves example shown above, shows the four different regions of operation for a JFET and these are given as:

- Ohmic Region – When VGS = 0 the depletion layer of the channel is very small and the JFET acts like a voltage controlled resistor.

- Cut-off Region – This is also known as the pinch-off region were the Gate voltage, VGS is sufficient to cause the JFET to act as an open circuit as the channel resistance is at maximum.
- Saturation or Active Region – The JFET becomes a good conductor and is controlled by the Gate-Source voltage, (VGS) while the Drain-Source voltage, (VDS) has little or no effect.
- Breakdown Region – The voltage between the Drain and the Source, (VDS) is high enough to causes the JFET's resistive channel to break down and pass uncontrolled maximum current.

Transfer characteristics

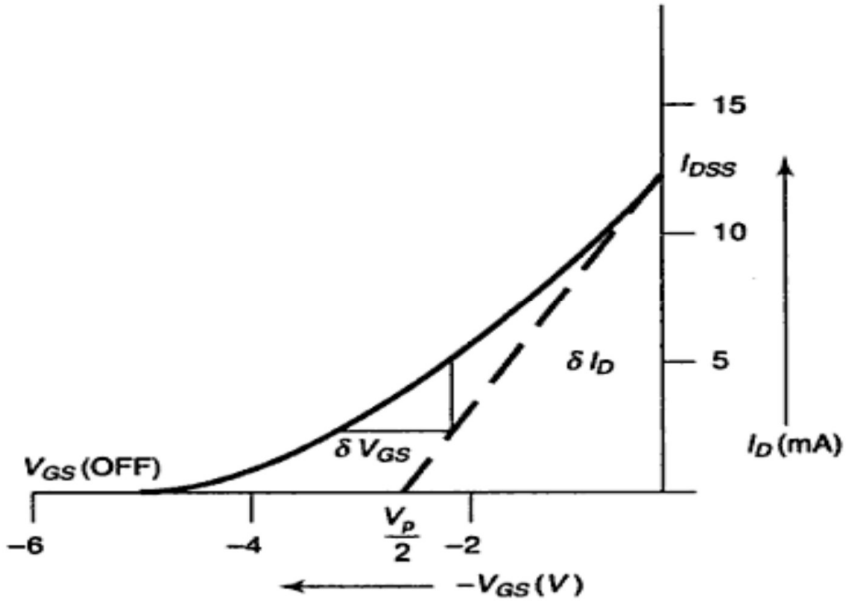

Fig:3.1.5 Transfer Characteristics of N-Channel JFET

The characteristics curves for a P-channel junction field effect transistor are the same as those above, except that the Drain current ID decreases with an increasing positive Gate-Source voltage, VGS.

The Drain current is zero when VGS = VP. For normal operation, VGS is biased to be somewhere between VP and 0. Then can calculate the Drain current, ID for any given bias point in the saturation or active region.

Drain current in the active region.

$$I_D = I_{DSS}\left[1-\frac{V_{GS}}{V_P}\right]^2$$

Note that the value of the Drain current will be between zero (pinch-off) and IDSS(maximum current). By knowing the Drain current ID and the Drain-Source voltage VDSthe resistance of the channel (ID) is given as:

Drain-Source channel resistance.

$$R_{DS} = \frac{\Delta V_{DS}}{\Delta I_D} = \frac{1}{g_m}$$

Where: gm is the "transconductance gain" since the JFET is a voltage controlled device and which represents the rate of change of the Drain current with respect to the change in Gate-Source voltage.

JFET Applications

- JFET is used as a switch.
- JFET is used as a chopper.
- Used as an amplifier.
- Used as a buffer.
- Used in the oscillatory circuits because of its low frequency drift.
- Used in communication equipments, such as FM and TV receivers because of their low modulation distortion.
- Used as voltage controlled resistors in operational amplifiers.
- JFETs are used in cascade amplifiers and in RF amplifiers.