4.4 SWITCHES FOR DAC

The Switches which connects the digital binary input to the nodes of a D/A converter is an electronic switch. Although switches can be made of using diodes, bipolar junction Transistors, Field Effect transistors or MOSFETs, there are four main configurations used as switches for DACs. They are

- Switches using overdriven Emitter Followers.
- Switches using MOS Transistor- Totem pole MOSFET Switch and CMOS Inverter
- Switch.
- CMOS switch for Multiplying type DACs.
- CMOS Transmission gate switches.

These configurations are used to ensure the high speed switching operations for different types of DACs.

SWITCHES USING OVERDRIVEN EMITTER FOLLOWERS

The bipolar transistors have a negligible resistance when they are operated in saturation. The bipolar transistor operating in saturation region indicates a minimum resistance and thus represents ON condition. When they are operating in cut-off region indicates a maximum resistance and thus represents OFF condition.

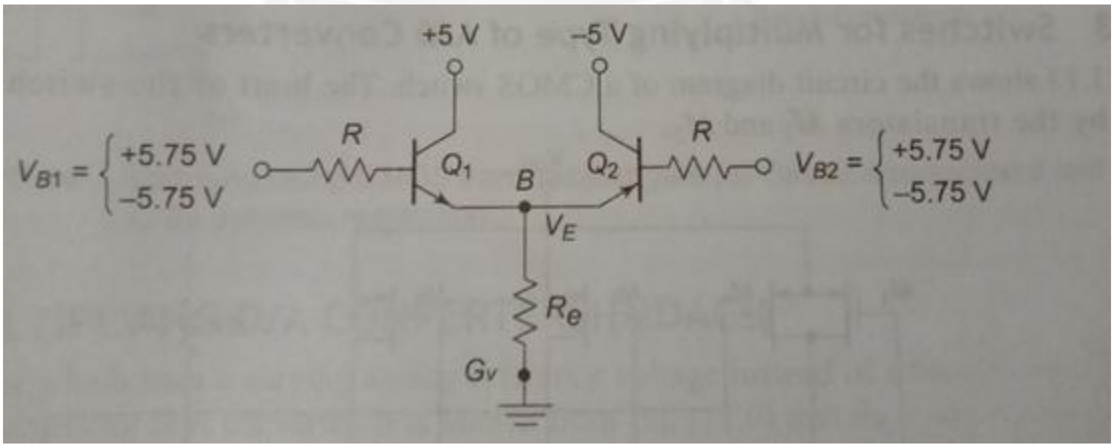

Figure 4.4.1 Switches for D/A converters using overdriven emitter followers

[source:"Linear Integrated Circuits"by S.Salivahanan& V.S. Kanchana Bhaskaran, Page-461]

The circuit shown in figure 4.4.1 is the arrangement of two transistors connected as emitter followers. A silicon transistor operating in saturation will have an offset voltage of 0.2V dropped across them. To have a zero offset voltage condition, the transistors must be overdriven because the saturation factor becomes negative. The two transistors Q1 (NPN) and Q2 (PNP) acts as a double pole switch. The bases of the transistors are driven by +5.75V and -5.75V.

Case 1:

When VB1 = VB2 = +5.75V, Q1 is in saturation and Q2 is OFF. And VE ≈ 5V with VBE1 = VBE2 = 0.75V

Case 2:

When VB1 = VB2 = -5.75V, Q2 is in saturation and Q1 is OFF. And VE ≈ - 5V with VBE1 = VBE2 = 0.75V

Thus the terminal B of the resistor Re is connected to either -5V or +5V depending on the input bit.

SWITCHES USING MOS TRANSISTOR

i) TOTEM POLE MOSFET SWITCH

As shown in the figure 4.4.2, the totem pole MOSFET Switch is connected in series with resistors of R-2R network. The MOSFET driver is connected to the inverting terminal of the summing op-amp.

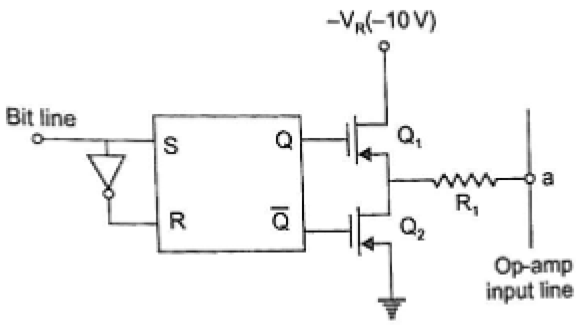

Figure 4.4.2. Totem pole MOSFET Switch

[source:"Linear Integrated Circuits"by S.Salivahanan& V.S. Kanchana Bhaskaran, Page-462]

The complementary outputs Q and Q drive the gates of the MOSFET M_1 and M_2 respectively. The SR flip flop holds one bit of digital information of the binary word under conversion. Assuming the negative logic (-5V for logic 1 and +5V for logic 0) the operation is given as two cases.

Case 1:

When the bit line is 1 with S=1 and R=0 makes Q=1 and Q =0. This makes the transistor M1 ON, thereby connecting the resistor R to reference voltage -VR. The transistor M2 remains in OFF condition.

Case 2:

When the bit line is 0 with S=0 and R=1 makes Q=0 and Q =1. This makes the transistor M2 ON, thereby connecting the resistor R toGround. The transistor M1 remains inOFF condition.

ii) CMOS INVERTER SWITCH

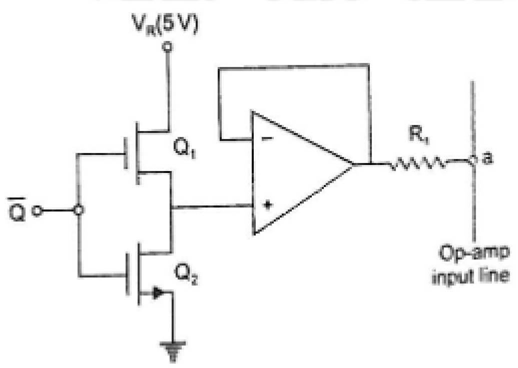

Figure 4.4.3 CMOS Inverter Switch

[source:"Linear Integrated Circuits"by S.Salivahanan& V.S. Kanchana Bhaskaran, Page-462]

The figure 4.4.3 of CMOS inverter is shown here. It consists of a CMOS inverter connected with an op-amp acting as a buffer. The buffer drives the resistor R with very low output impedance.Assuming positive logic (+5V for logic 1 and 0V for logic 0), the operation can be explained in two cases.

Case1:

When the complement of the bit line Q is low, M_1 becomes ON connecting V_R to the non- inverting input of the op-amp. This drives the resistor R HIGH.

Case2:

When the complement of the bit line Q is high, M_2 becomes ON connecting Ground to the non- inverting input of the op-amp. This pulls the resistor R LOW (to ground).

CMOS SWITCH FOR MULTIPLYING TYPE DACS

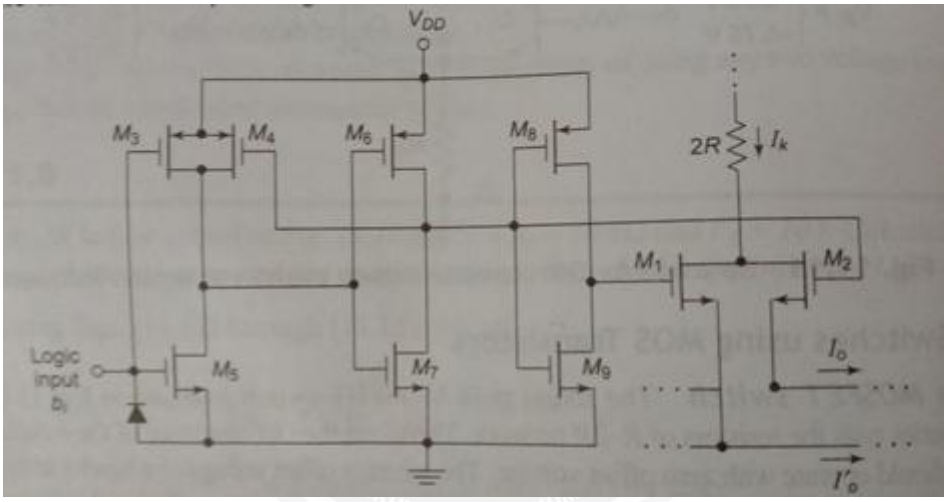

Figure 4.4.4 CMOS switch for Multiplying type DACs

[source:"Linear Integrated Circuits"by S.Salivahanan& V.S. Kanchana Bhaskaran, Page-462]

The CMOS switch for Multiplying type DACs is shown in figure 4.4.4. The heart of the switching element is formed by transistors M_1 and M_2. The remaining transistors accept TTL or CMOS compatible logic inputs and provides the anti-phase gate drives for the transistors M_1 and M_2. The operation for the two cases is as follows.

Case 1:

When the logic input is 1, M_1 is ON and M_2 is OFF. Thus current IK is diverted to Io bus.

Case 2:

When the logic input is 0, M_2 is ON and M_1 is OFF. Thus current IK is diverted to Io bus.

CMOS TRANSMISSION GATE SWITCHES

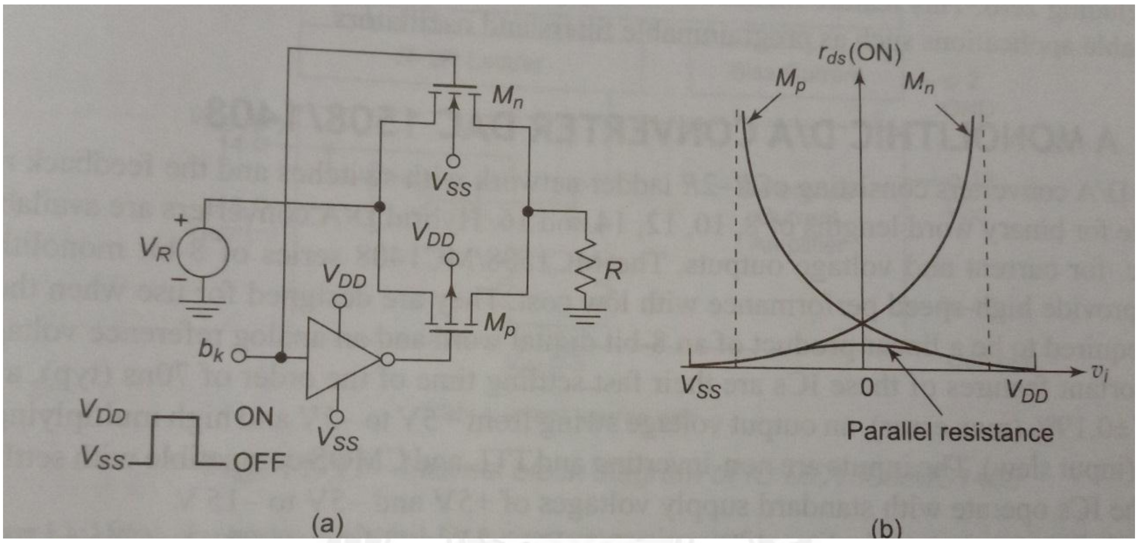

Figure 4.4.5a).Switches using CMOS transmission gate and

Figure 4.4.5 b) is its dynamic characteristics

[source:"Linear Integrated Circuits"by S.Salivahanan& V.S. Kanchana Bhaskaran, Page-463]

The disadvantage of using individual NMOS and PMOS transistors are threshold voltage drop (NMOS transistor passing only minimum voltage of V_R- V_{TH} and PMOS transistor passing minimum voltage of V_{TH}). This is eliminated by using transmission gates which uses a parallel connection of both NMOS and PMOS. The arrangement shown in figure 4.4.5 a) can pass voltages from VR to 0V acting as a ideal switch. The following cases explain the operation.

Case 1:

When the bit-line bk is HIGH, both transistors Mn and Mp are ON, offering low resistance over the entire range of bit voltages.

Case 2:

When the bit-line bk is LOW, both the transistors are OFF, and the signal transmission is inhibited (Withdrawn).

Figure 4.4.5 b) shows the dynamic characteristics.Thus the NMOS offers low resistance in the lower portion of the signal and PMOS offers low resistance in the upper portion of the signal. As a combination, they offer a low parallel resistance throughout the operating range of voltage. Wide varieties of these kinds of switches were available. Example: CD4066 and CD4051.